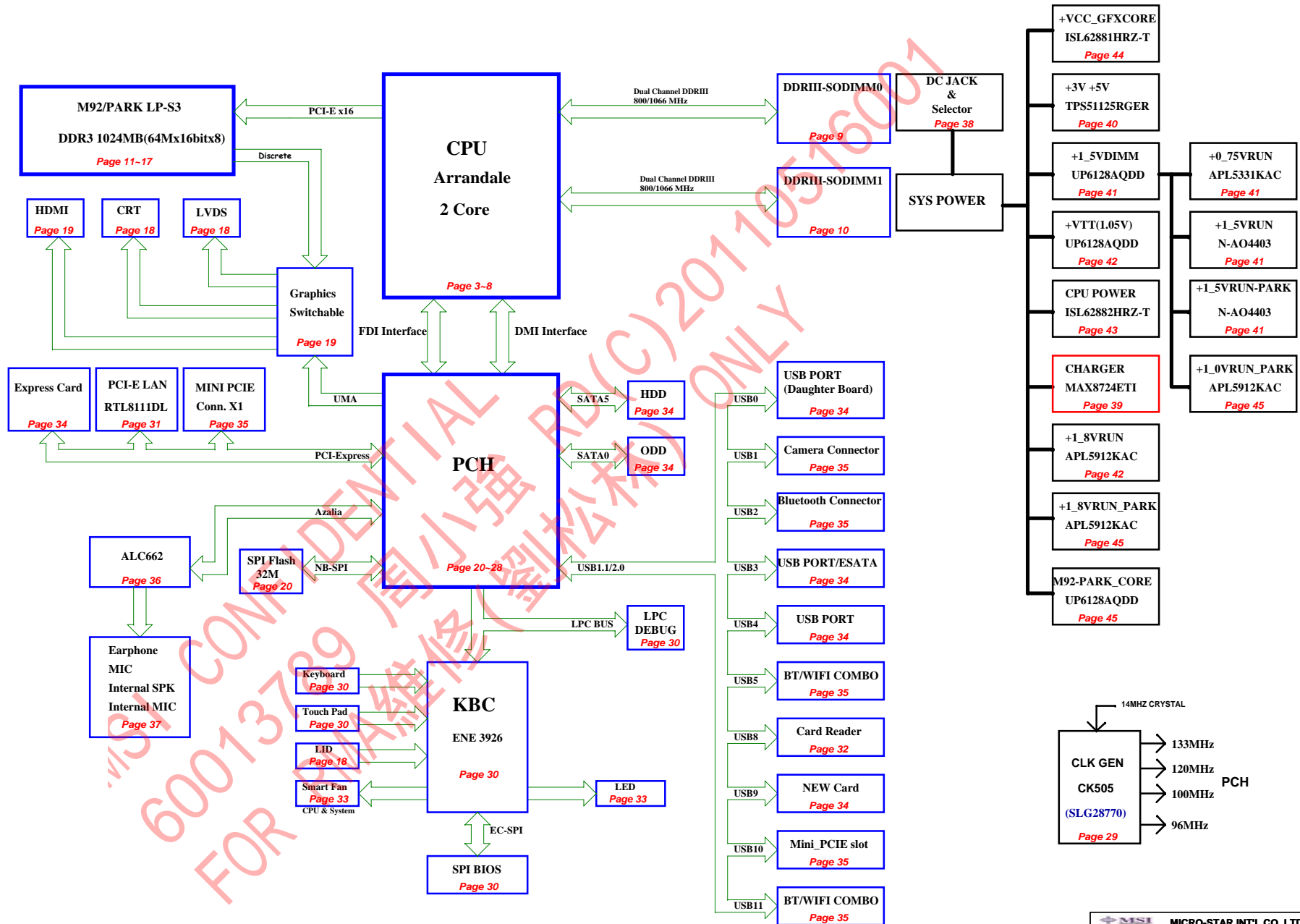


Calpella Platform

Page	Description
01	BLOCK DIAGRAM
02	PLATFORM
03	PROCESSOR-1 (HOST BUS)
04	PROCESSOR-2 (DDR3)
05	PROCESSOR-3 (POWER)
06	PROCESSOR-4 (GRAPHICS POWER)
07	PROCESSOR-5 (GND)
08	PROCESSOR-6 (RESERVE)
09	DDR3 SODIMM 0
10	DDR3 SODIMM 1
11	M92/Park-Sx (Host_LVDS)
12	M92/Park-Sx (Main_IO)
13	M92/Park-Sx (Power&GND)
14	M92/Park-Sx (DP_Power; Straps)
15	M92/Park-Sx (MEM_Interface)
16	DDR3 (64MX16bit)
17	DDR3 (64MX16bit)
18	CRT&LVDS
19	SWITCH&HDMI
20	PCH-1 (HDA, JTAG, SATA)
21	PCH-2 (PCI-E, SMBUS, CLK)
22	PCH-3 (DMI, FDI, GPIO)
23	PCH-4 (LVDS, DDI)
24	PCH-5 (PCI, USB, NVRAM)
25	PCH-6 (GPIO, VSS, NCTF, RSVD)
26	PCH-7 (POWER)
27	PCH-8 (POWER)
28	PCH-9 (GND)
29	Clock Generator (SL28770ELC)
30	KBC/EC/uP (KB3926)
31	PCIE 10/100/1000 LAN (RTL8111DL)
32	Cardreader (UB6250)
33	FAN, Launch board
34	HDD, CDROM, USB, NEWCARD, ESATA
35	MINIPIC, CAMERA, BLUETOOTH, SW
36	CODEC (ALC662) & Amp
37	SPK & HP & MIC
38	M_Battery select
39	M_Battery Charger
40	M_System Power
41	SMDDR_VTERM/1_5VRUN
42	VTT POWER, +1.8VRUN
43	M_CPU power
44	M_Graphic Core
45	M92/Park power
46	SCREW/ME
47	88A USB BOARD
48	88B_Touch Pad Board
49	EMI
50	Power ON Sequency
51	Power Down Sequence
52	Power MAP
53	Change History



SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

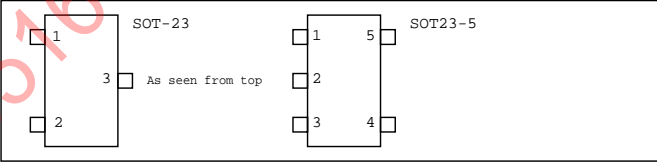
Voltage Rails

POWER PLANE	VOLTAGE	ACTIVE IN	DESCRIPTION
PWR_SRC	19V	S0,(S3-S5)	LAN DDRIII core PCH DDRIII command & control pull up. CPU core rail Graphics core rail (Dual Core only)
+5VALW	5V	S0,(S3-S5)	
+5VRUN	5V	S0	
+5VSUS	5V	S0	
+3VALW	3.3V	S0,(S3-S5)	
+3VSUS	3.3V	S0,(S3-S5)	
+3VRUN	3.3V	S0	
+1_5VDIMM	1.5V	S0,S3	
+1_5VRUN	1.5V	S0	
VTT	1.05V	S0	
+0_75VRUN	0.75V	S0	
+VCC_CORE	1.05V-1.1V	S0	
+VCC_GFXCORE	1.1V	S0	
M92S_VDD_CORE	0.95V	S0	GPU core power GPU PCIE power GPU DDR3 power GPU PCIE power GPU I/O and DAC power
+1_8VRUN_PARK	1.8V	S0	
+1_5VRUN_PARK	1.5V	S0	
+1_0VRUN_PARK	1.0V	S0	
VDDR3	3.3V	S0	

Net Naming Conventions

Suffix
= Active Low Signal
Prefix
H = Host
M = DDR Memory
TP = Test Point (does not connect anywhere else)

PCB Footprints



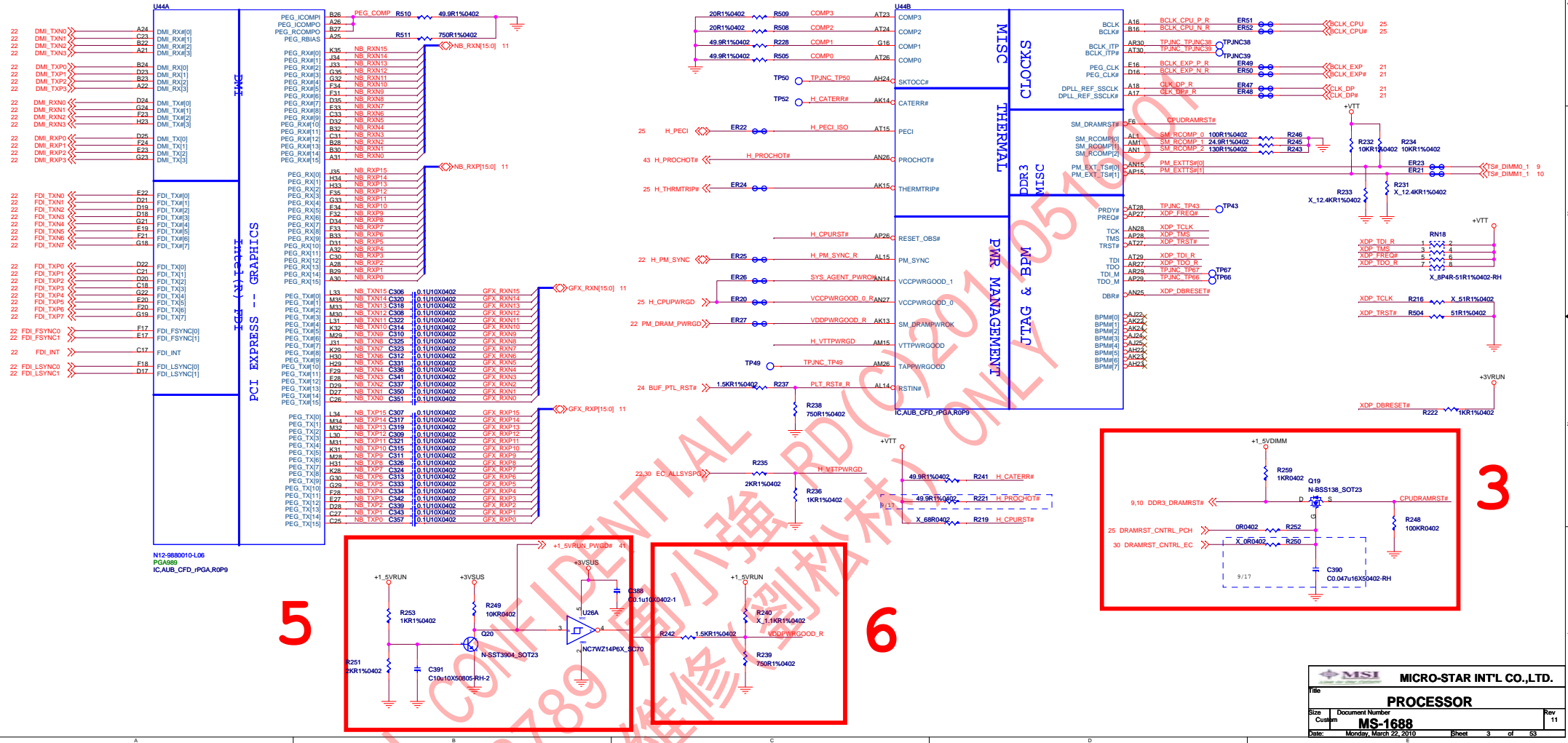
AC Mode

Power States	SLP_S3#	SLP_S4#	SLP_S5#	SLP_LAN#	+V*ALWAYS	+V*SUS	+V*RUN	CLK
S0 (Full on)	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S5 (Soft Off)	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF

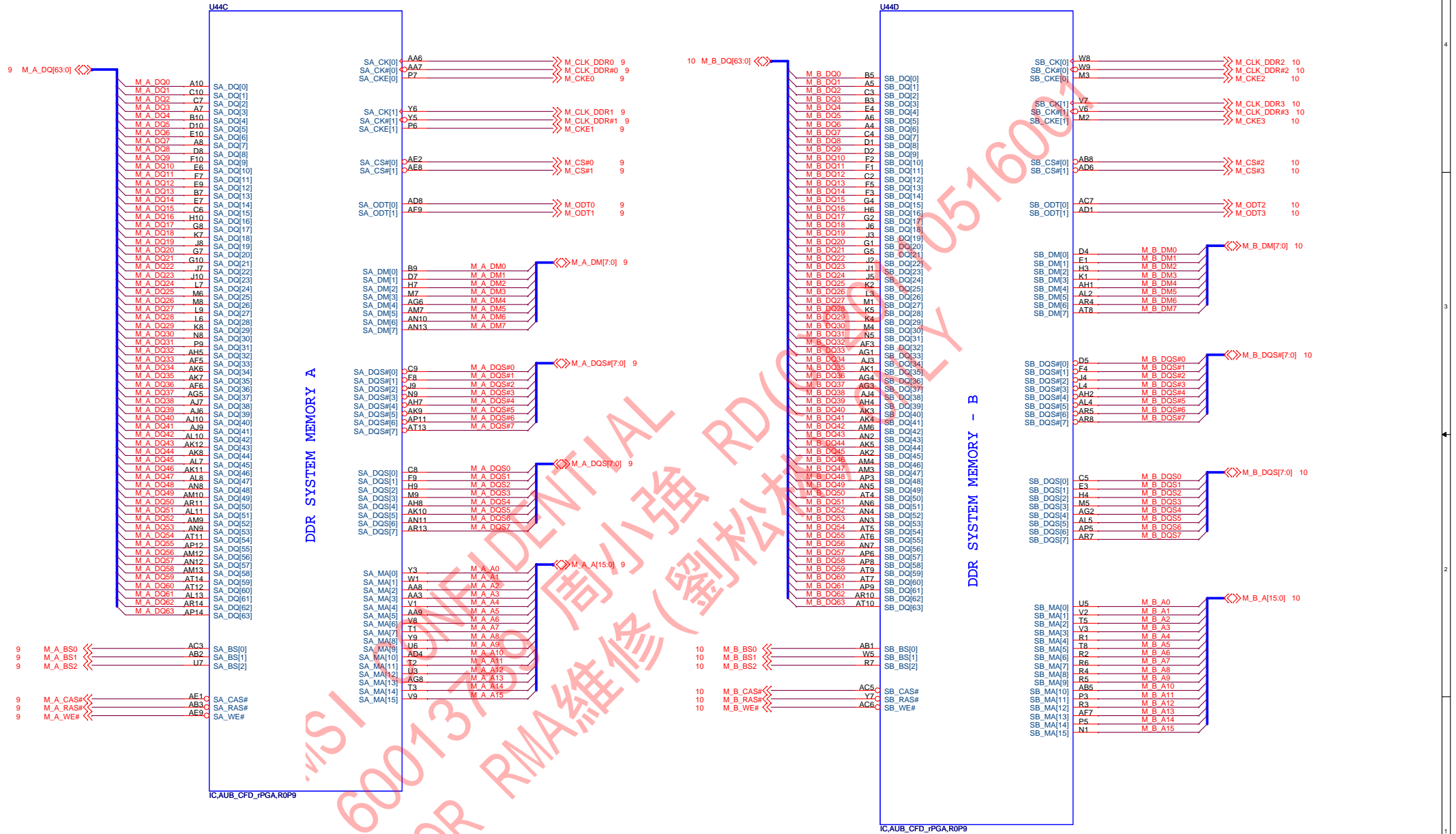
Battery Mode

Power States	SLP_S3#	SLP_S4#	SLP_S5#	SLP_LAN#	+V*ALWAYS	+V*SUS	+V*RUN	CLK
S0 (Full on)	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	HIGH	ON	OFF	OFF	OFF
S5 (Soft Off)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF

ARRANDALE PROCESSOR (CLK,MISC,JTAG)



ARRANDALE PROCESSOR (DDR3)



ARRANDALE PROCESSOR (POWER)

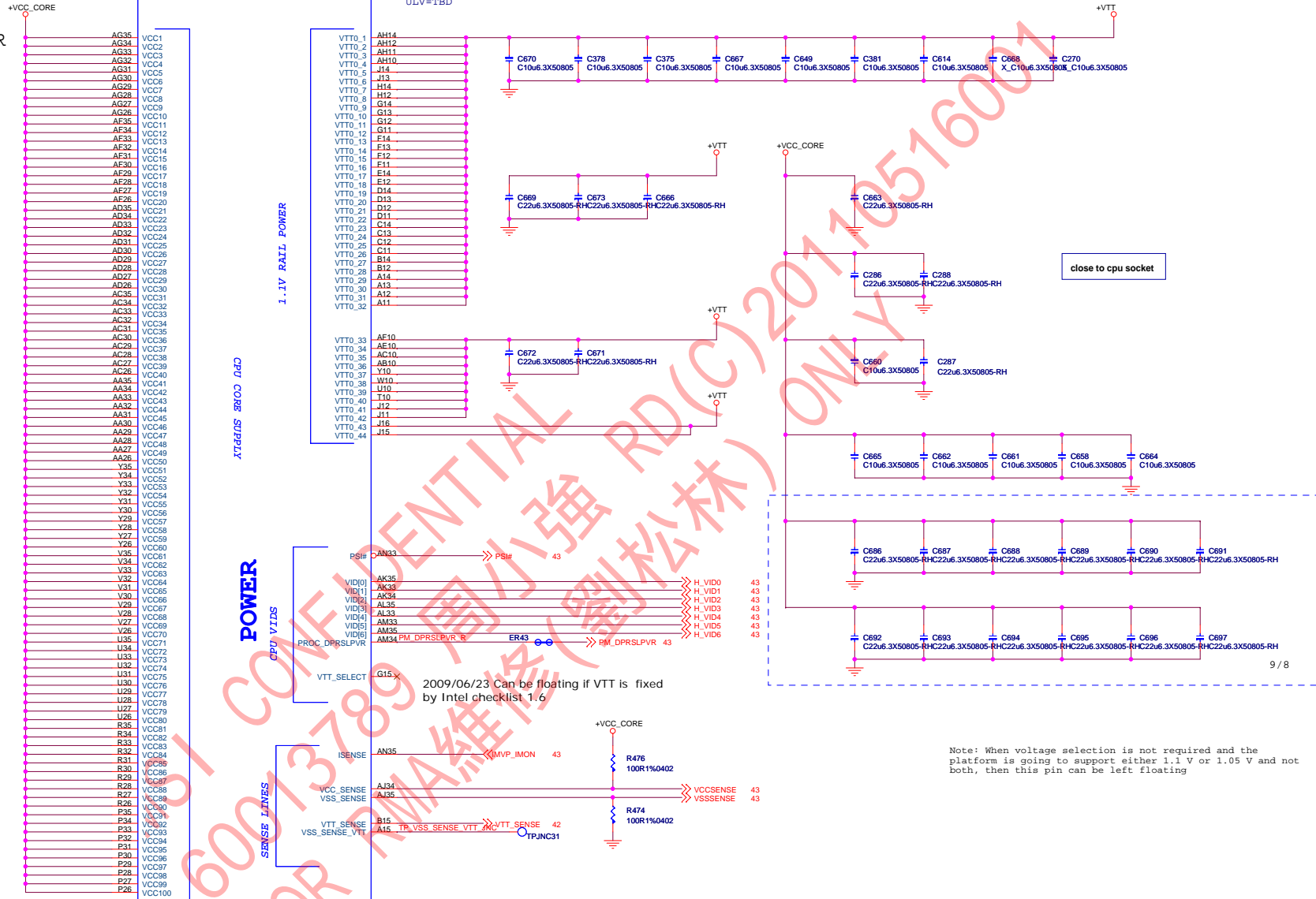
ARRANDALE:
SV=48A
LV=35A
ULV=27A

U44F

ARRANDALE:
SV=18A
LV=18A
ULV=TBD

PROCESSOR CORE POWER

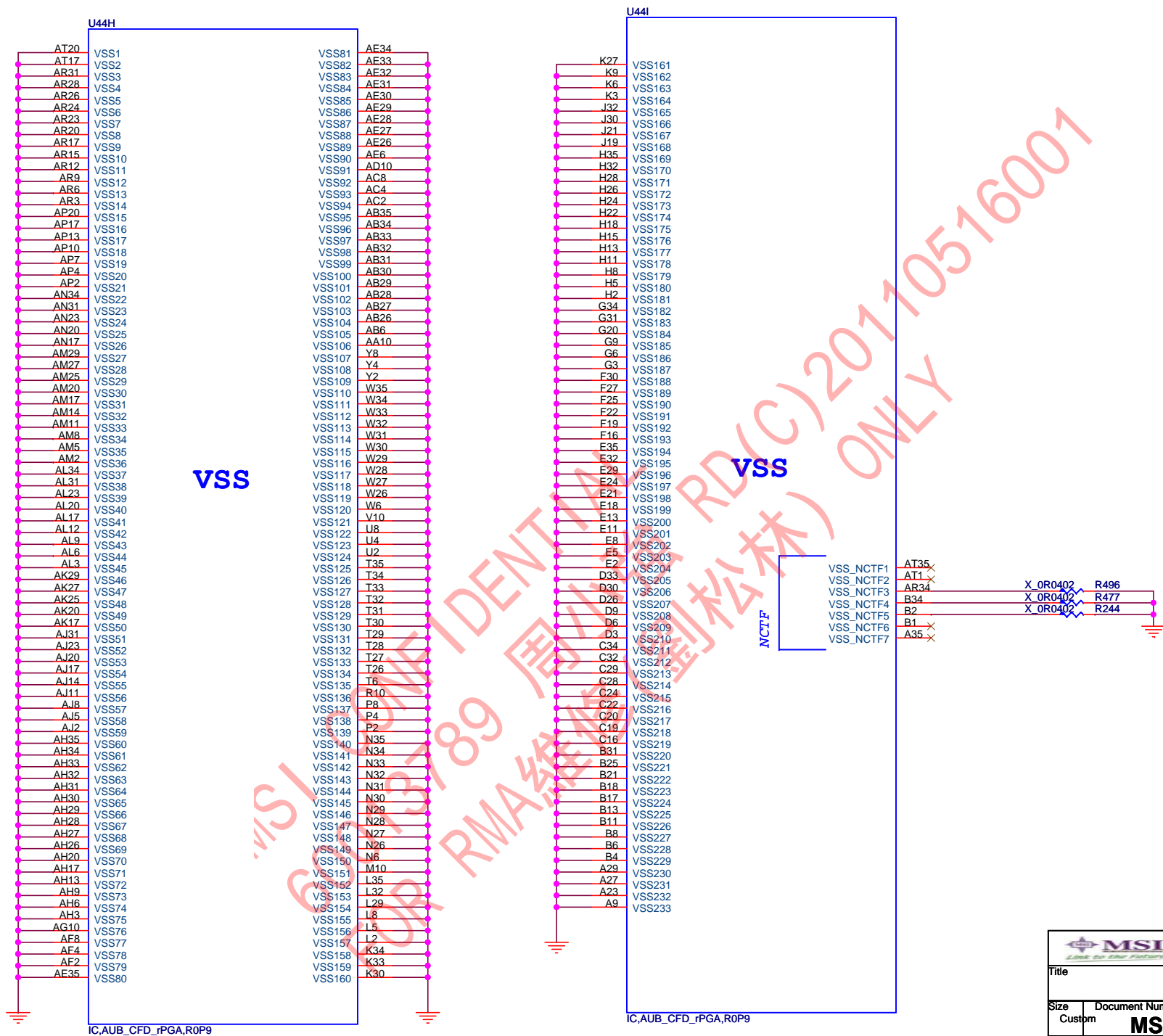
PROCESSOR CORE POWER



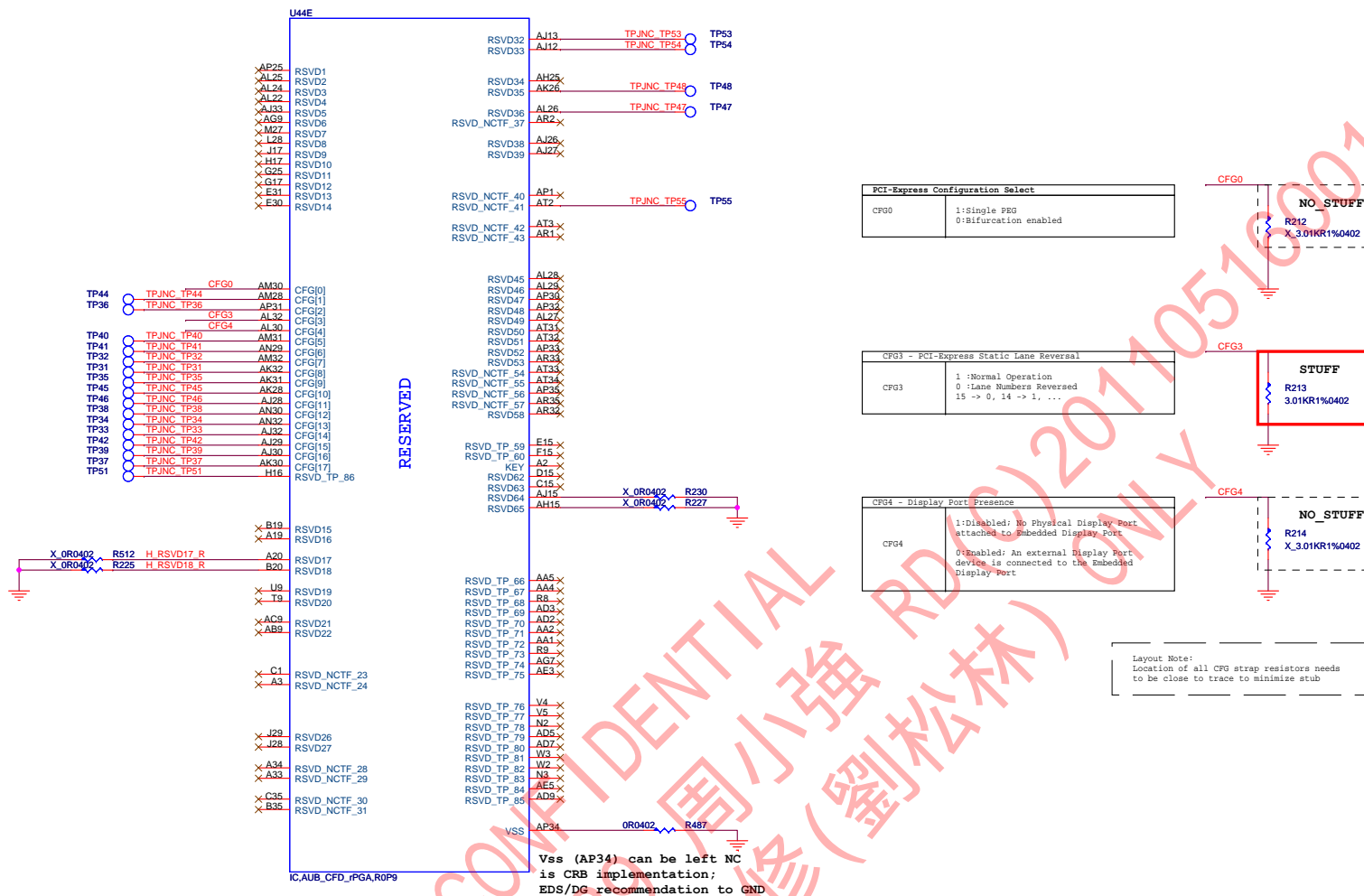
IC_AUB_CFD_IPGA_R0P9



ARRANDALE PROCESSOR (GND)



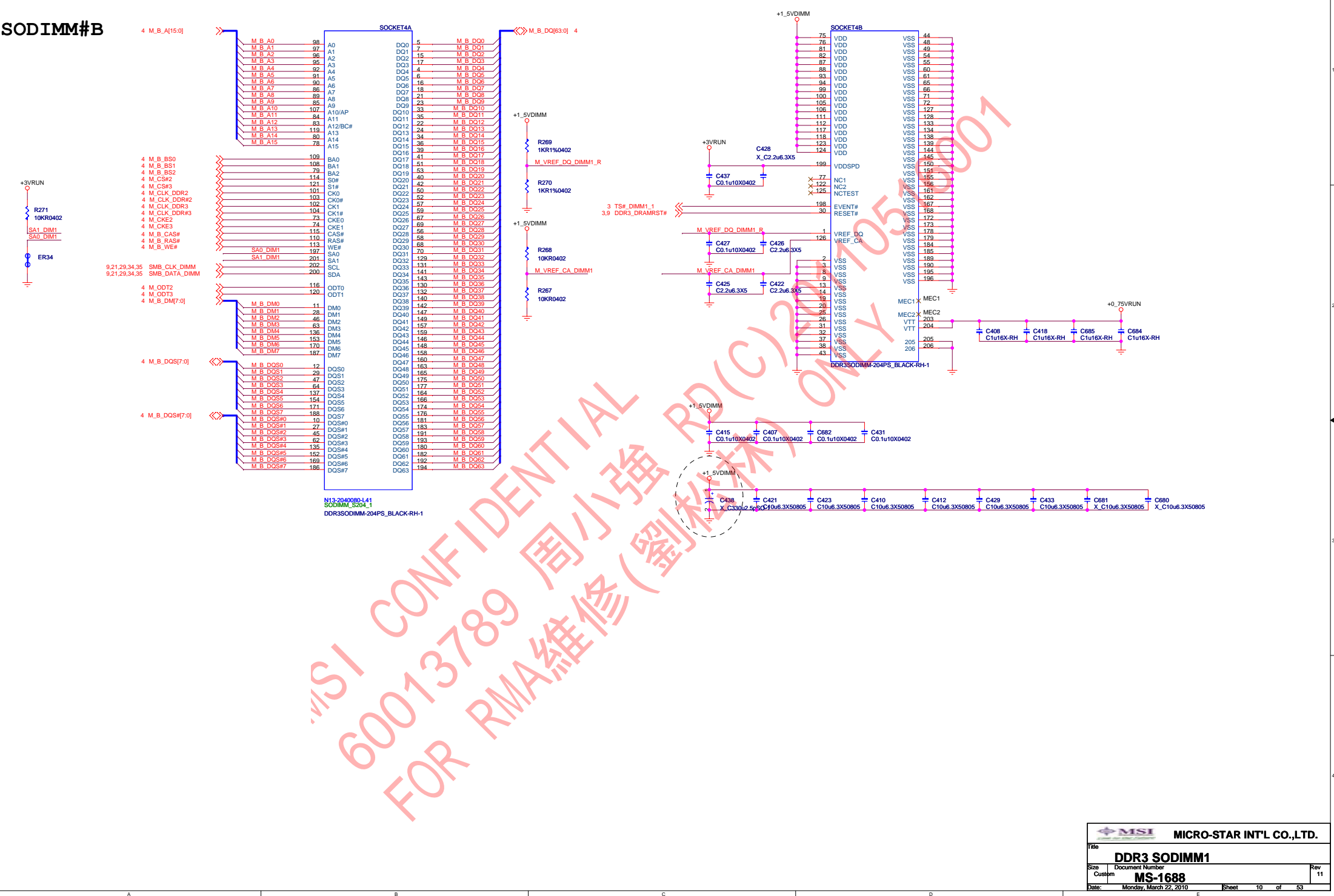
ARRANDALE PROCESSOR (RESERVED)

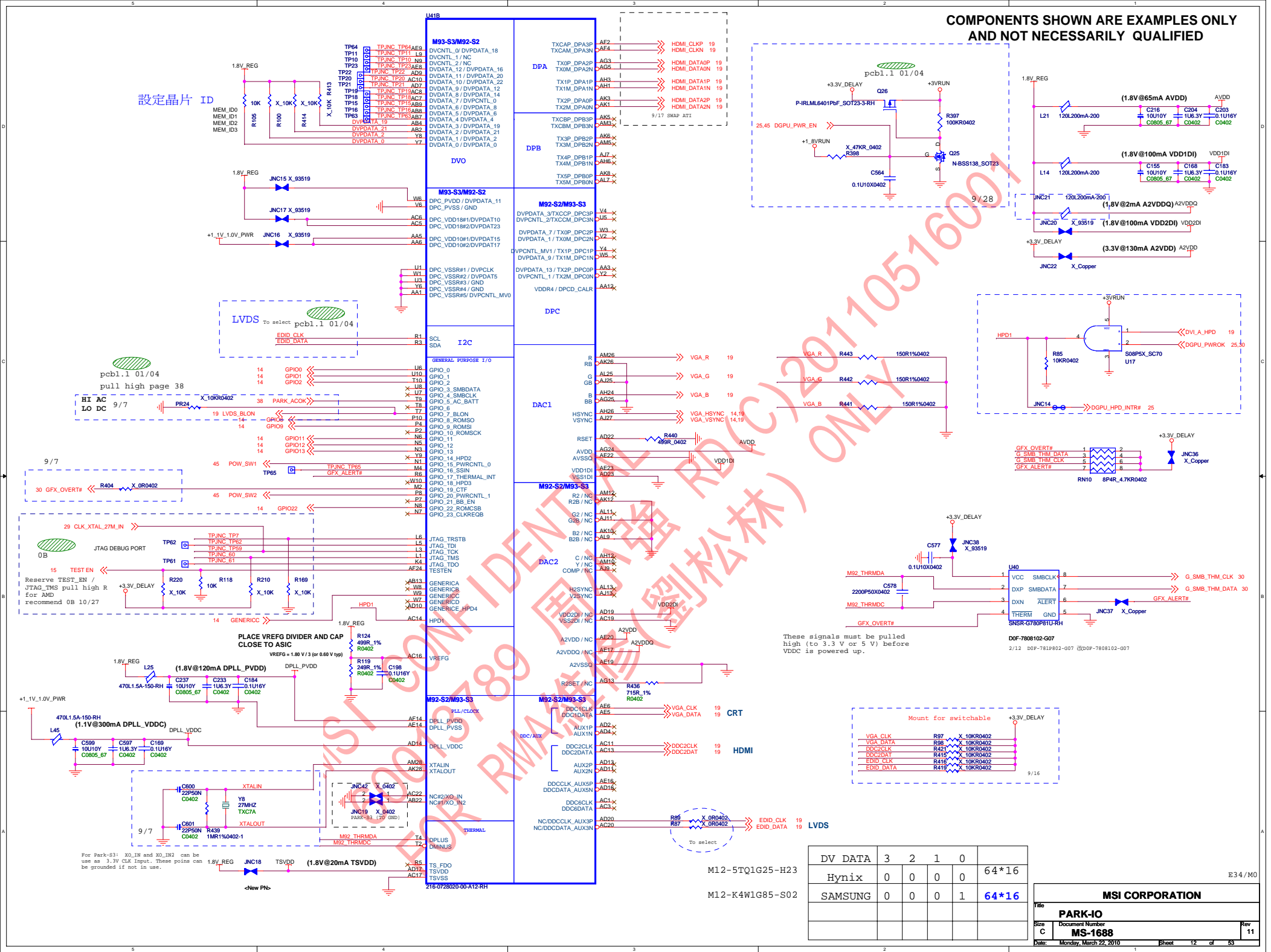


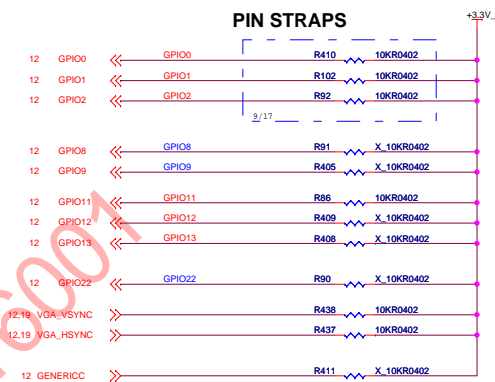
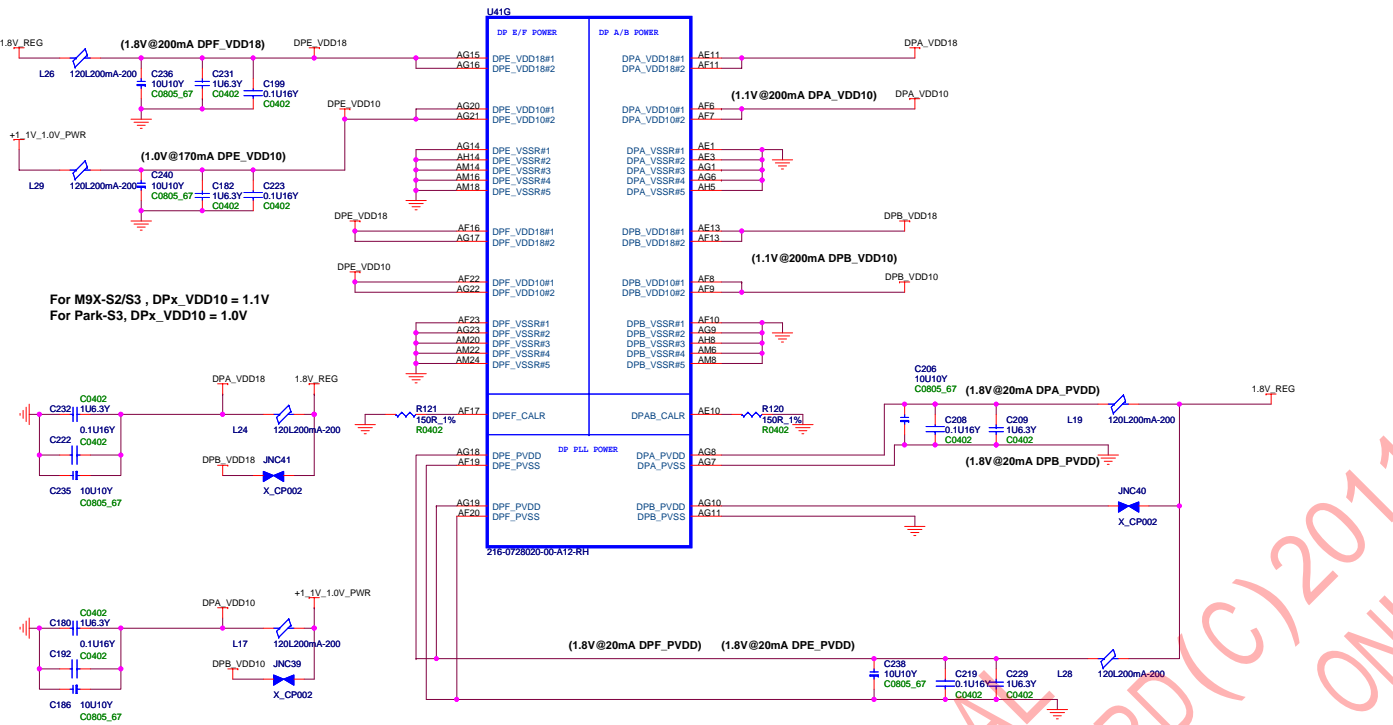
SODIMM#A



SODIMM#B







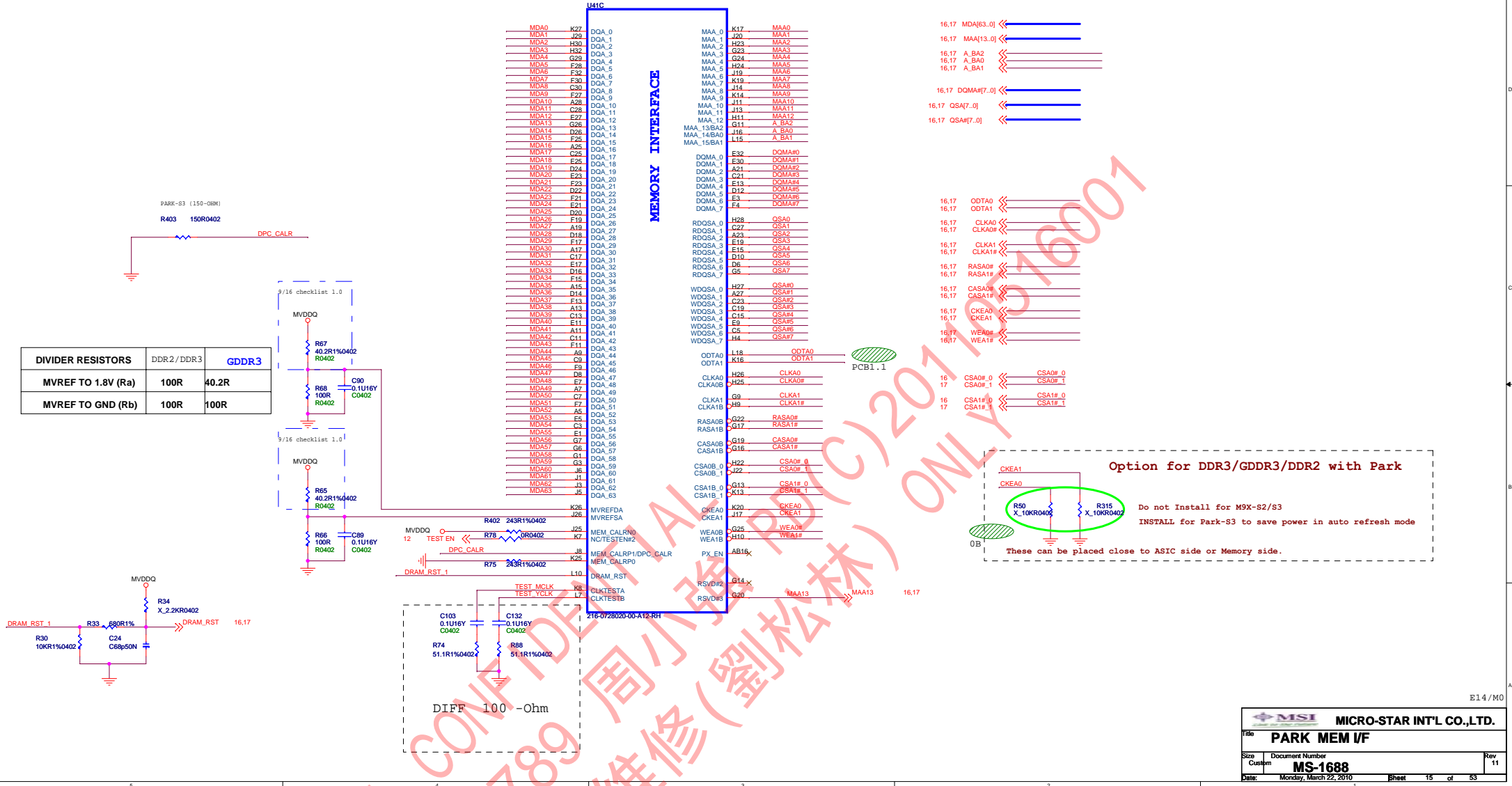
CONFIGURATION STRAPS			
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET			
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS (0= DO NOT INSTALL RESISTOR 1 = INSTALL 10K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE)
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	X
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X
BIF_GEN2_EN_A	GPIO2	PCIE GEN2 ENABLED	X
RSVD	GPIO8	VGA ENABLED	0
BIF_VGA_DIS	GPIO9		0
RSVD	GPIO21		0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	X
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	X X X
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	X
RSVD	GENERICC	AUD[1] AUD[0]	0
AUD[1]	HSYNC	0 0 No audio function	0
AUD[0]	VSXNC	0 1 Audio for DisplayPort and HDMI if dongle is detected	0
		1 0 Audio for DisplayPort only	1
		1 1 Audio for both DisplayPort and HDMI	X

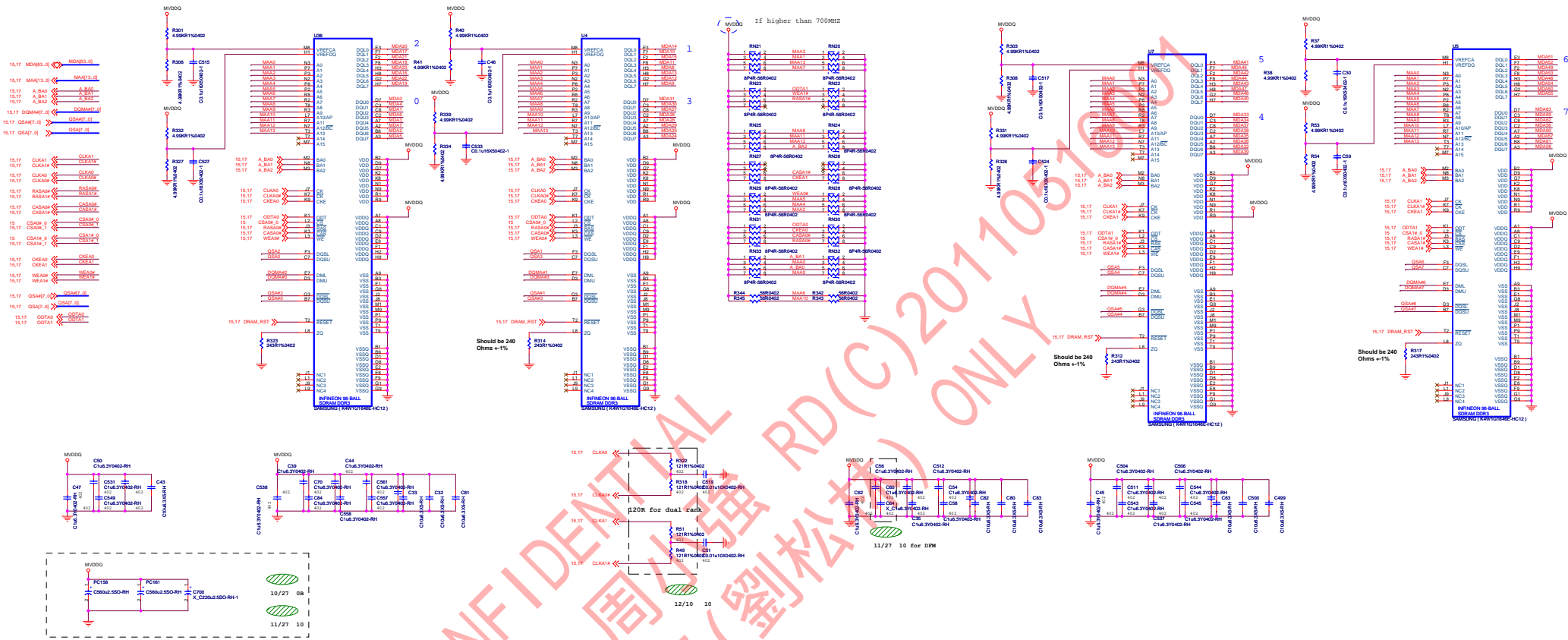
GPIO 13 12 11	
Size of the primary memory apertures	CONFIG[2:0]
128 MB	000
256 MB	001
64 MB	010
512 MB 1G MB	001

Due to memory management constraints, the aperture size should be the same size as the frame buffer for 64 MB, 128 MB and 256 MB. For frame buffers larger than 256 MB (e.g. 512 MB, 1 GB) the aperture size should be 256 MB.

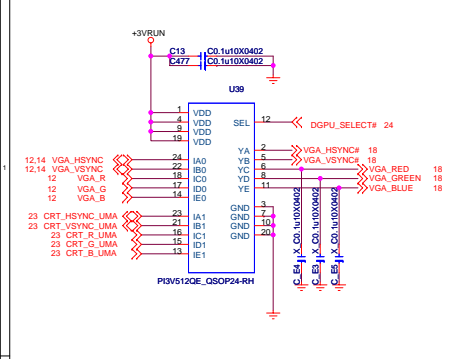
AMD RESERVED CONFIGURATION STRAPS	
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET	
H2SYNC	GENERICC
PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET	
GPIO21_BB_EN	

MSI CORPORATION			
Title	PARK-power straps		
Size	Document Number	Rev	11
Custom	MS-1688		
Date: Monday, March 22 2010	Sheet	14	of 53





CRT Switch

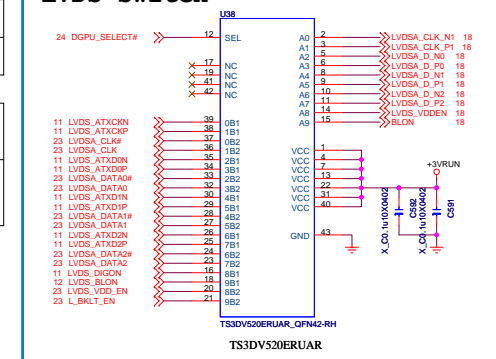


Logic Input

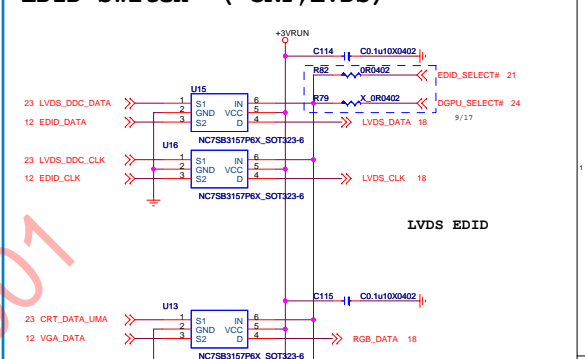
Logic Input	Function
0	S2 PORT
1	S1 PORT

BR-ADJ	
MXM only	1. MXM 2. EC
Switchable	1. MXM 2. iGPU 3. EC

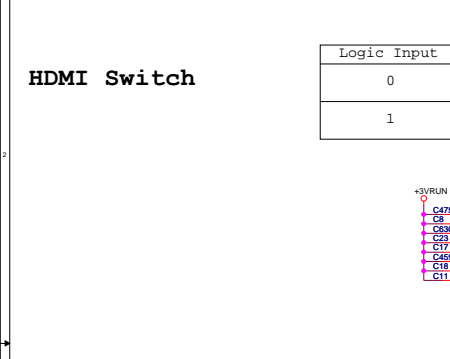
LVDS Switch



EDID Switch (CRT, LVDS)

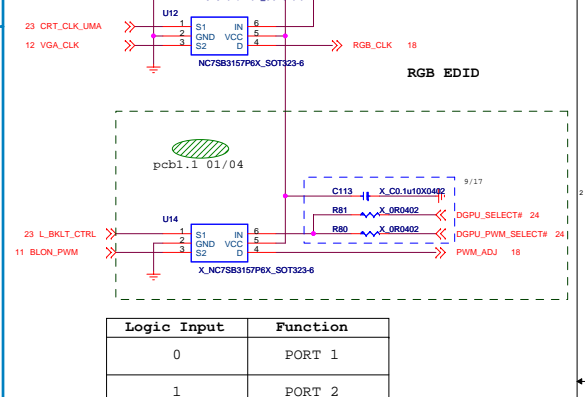
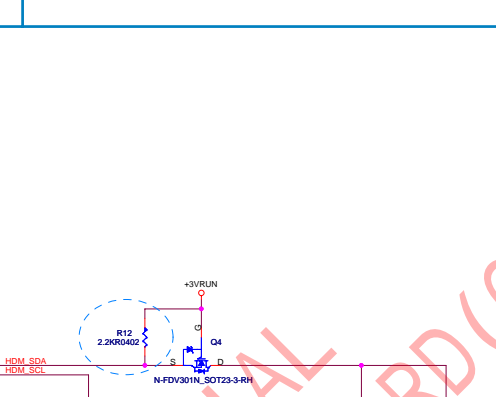


HDMI Switch

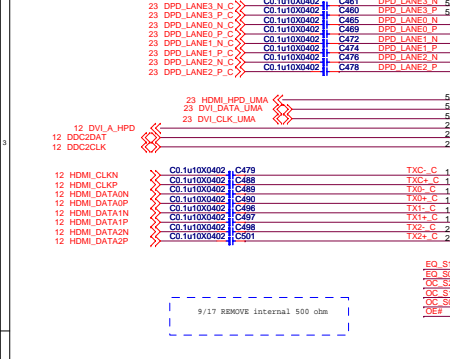


Logic Input

Logic Input	Function
0	B PORT
1	A PORT

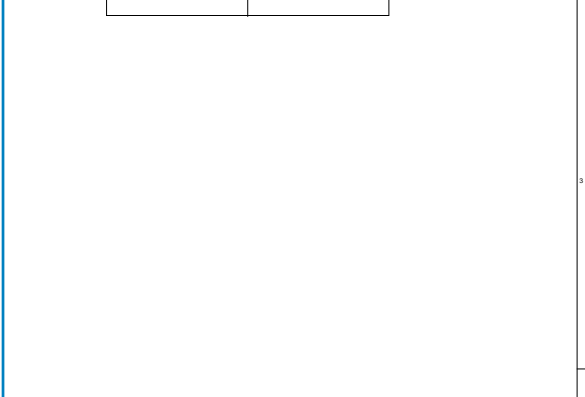
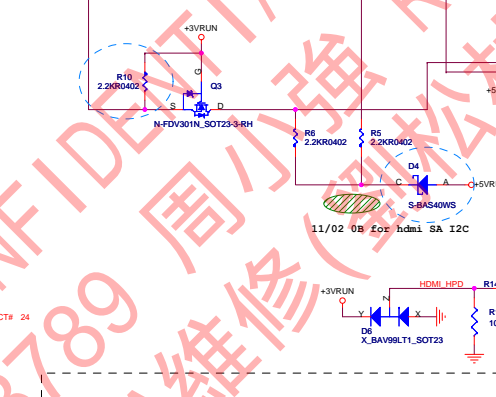


HDMI Switch

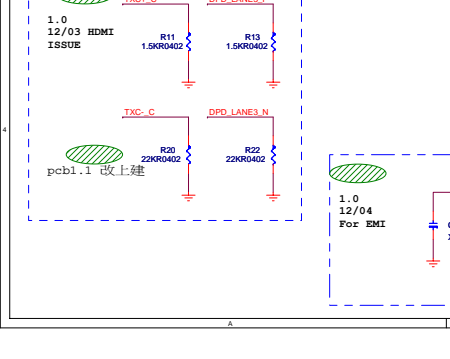


Logic Input

Logic Input	Function
0	B PORT
1	A PORT

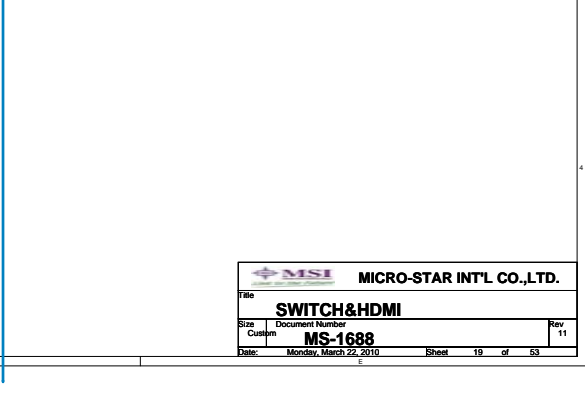
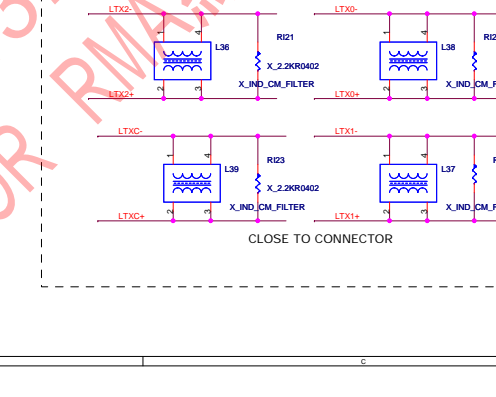


HDMI Switch



Logic Input

Logic Input	Function
0	B PORT
1	A PORT



9/16 QS之後的 版本只要R481 上件(TCK)

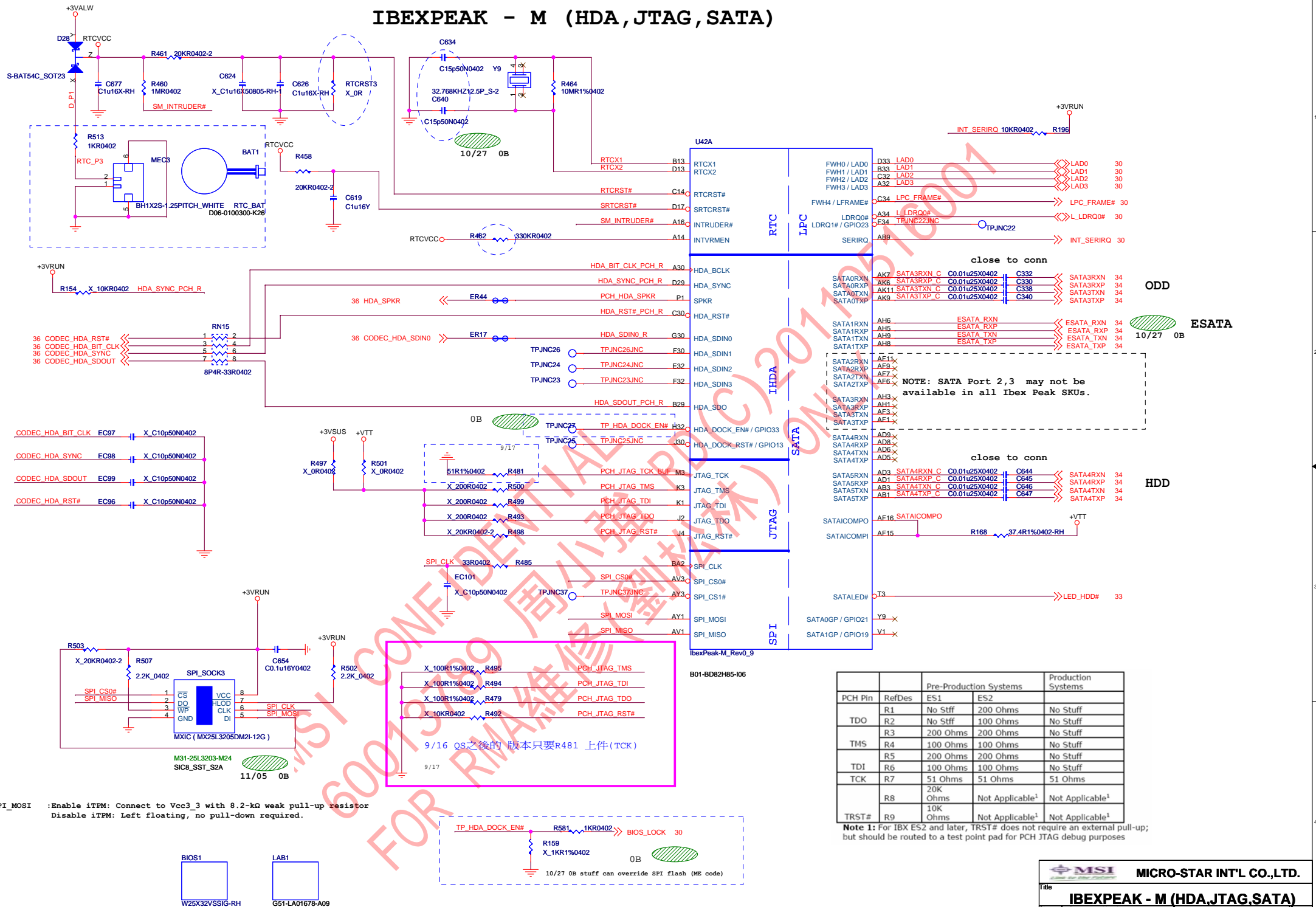
9/17

FOR RMA ONLY

TP_HDA_DOCK_EN# R581 1KR0402 >> BIOS_LOCK 30

R159 X_1KR1%0402 0B

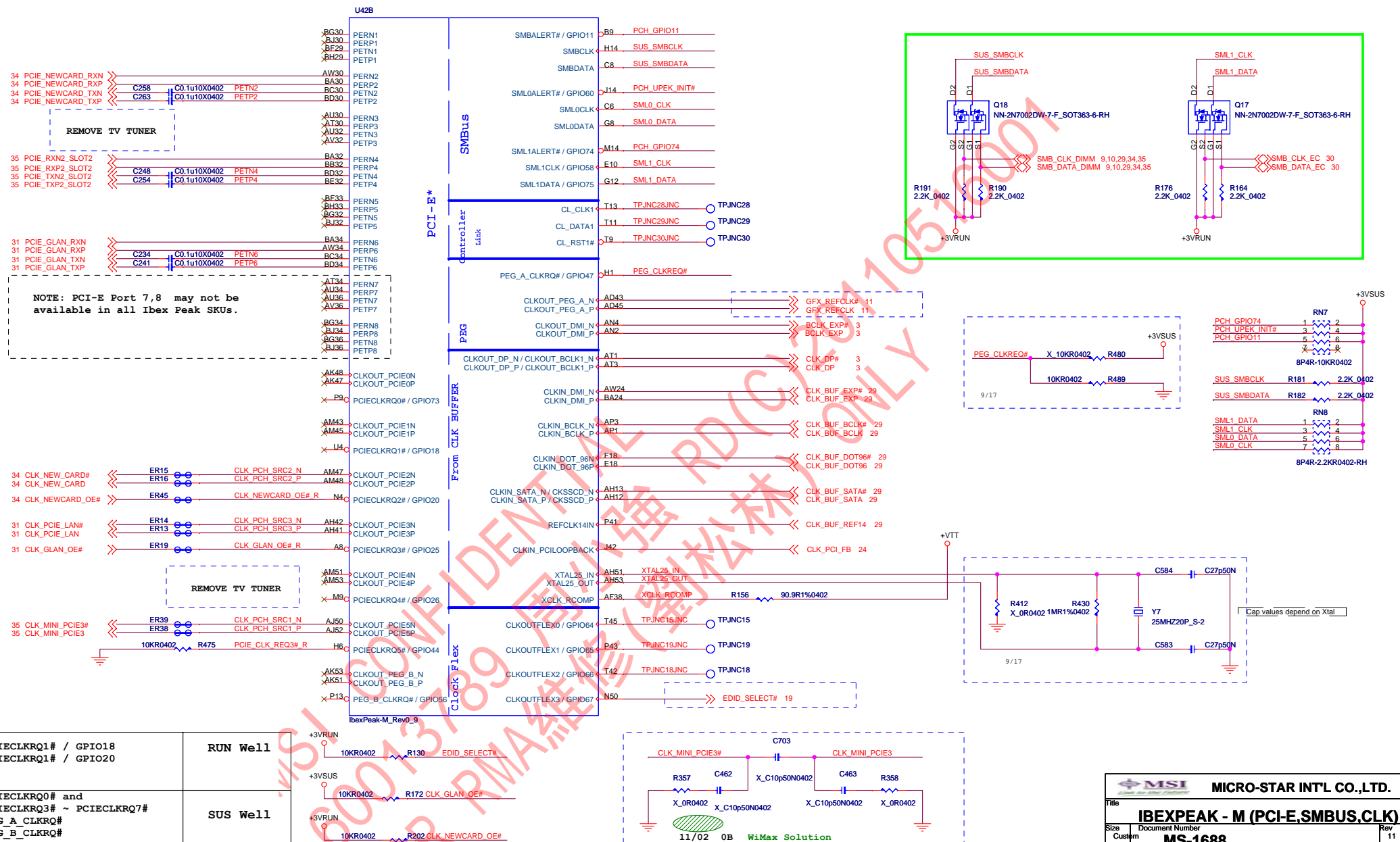
10/27 0B stuff can override SPI flash (ME code)



		Pre-Production Systems		Production Systems
PCH Pin	RefDes	ES1	ES2	
TDO	R1	No Stff	200 Ohms	No Stuff
	R2	No Stff	100 Ohms	No Stuff
	R3	200 Ohms	200 Ohms	No Stuff
TMS	R4	100 Ohms	100 Ohms	No Stuff
	R5	200 Ohms	200 Ohms	No Stuff
TDI	R6	100 Ohms	100 Ohms	No Stuff
TCK	R7	51 Ohms	51 Ohms	51 Ohms
TRST#	R8	20K Ohms	Not Applicable ³	Not Applicable ¹
	R9	10K Ohms	Not Applicable ³	Not Applicable ¹

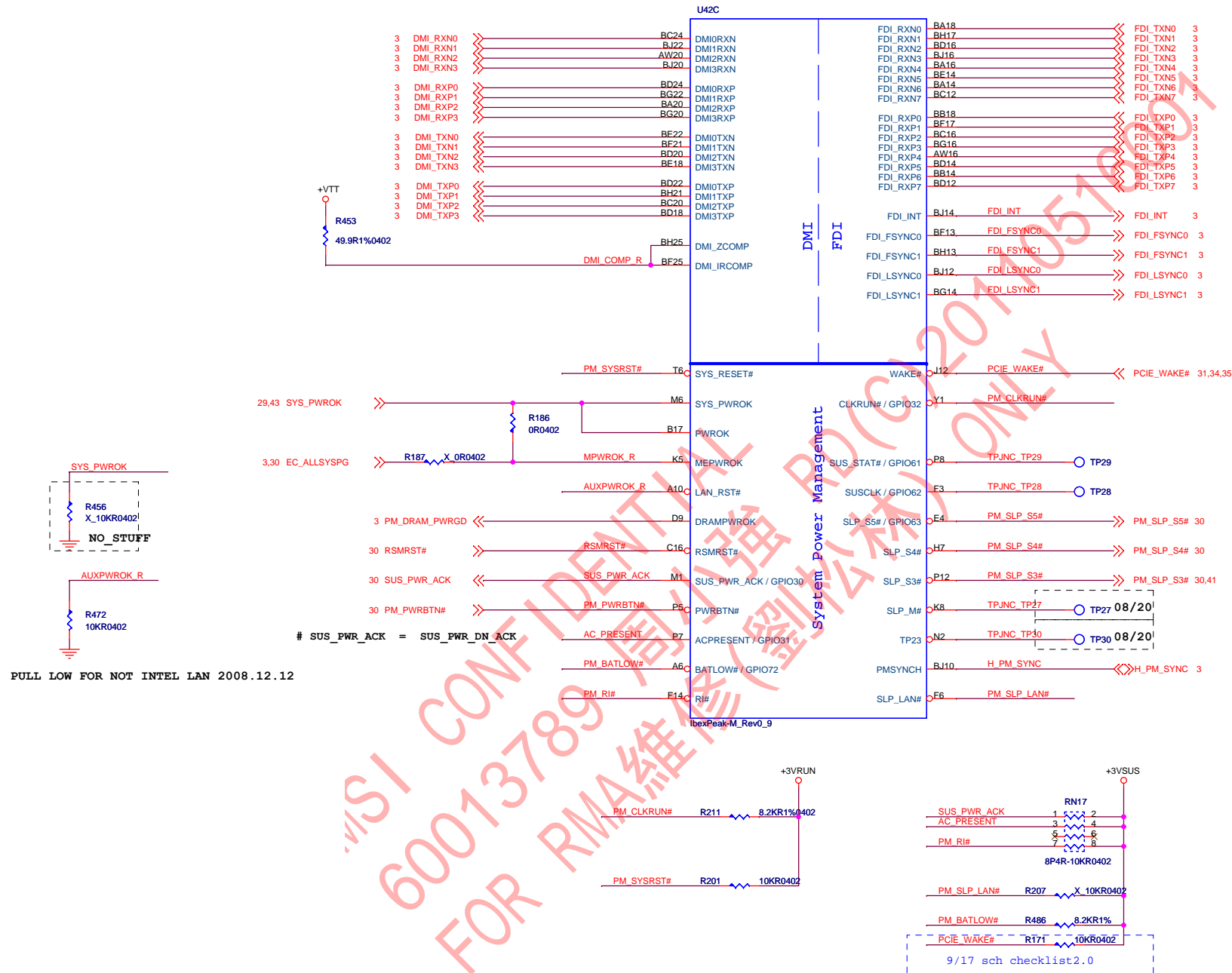
Note 1: For IBX ES2 and later, TRST# does not require an external pull-up; but should be routed to a test point pad for PCH JTAG debug purposes

IBEXPEAK - M (PCI-E, SMBUS, CLK)

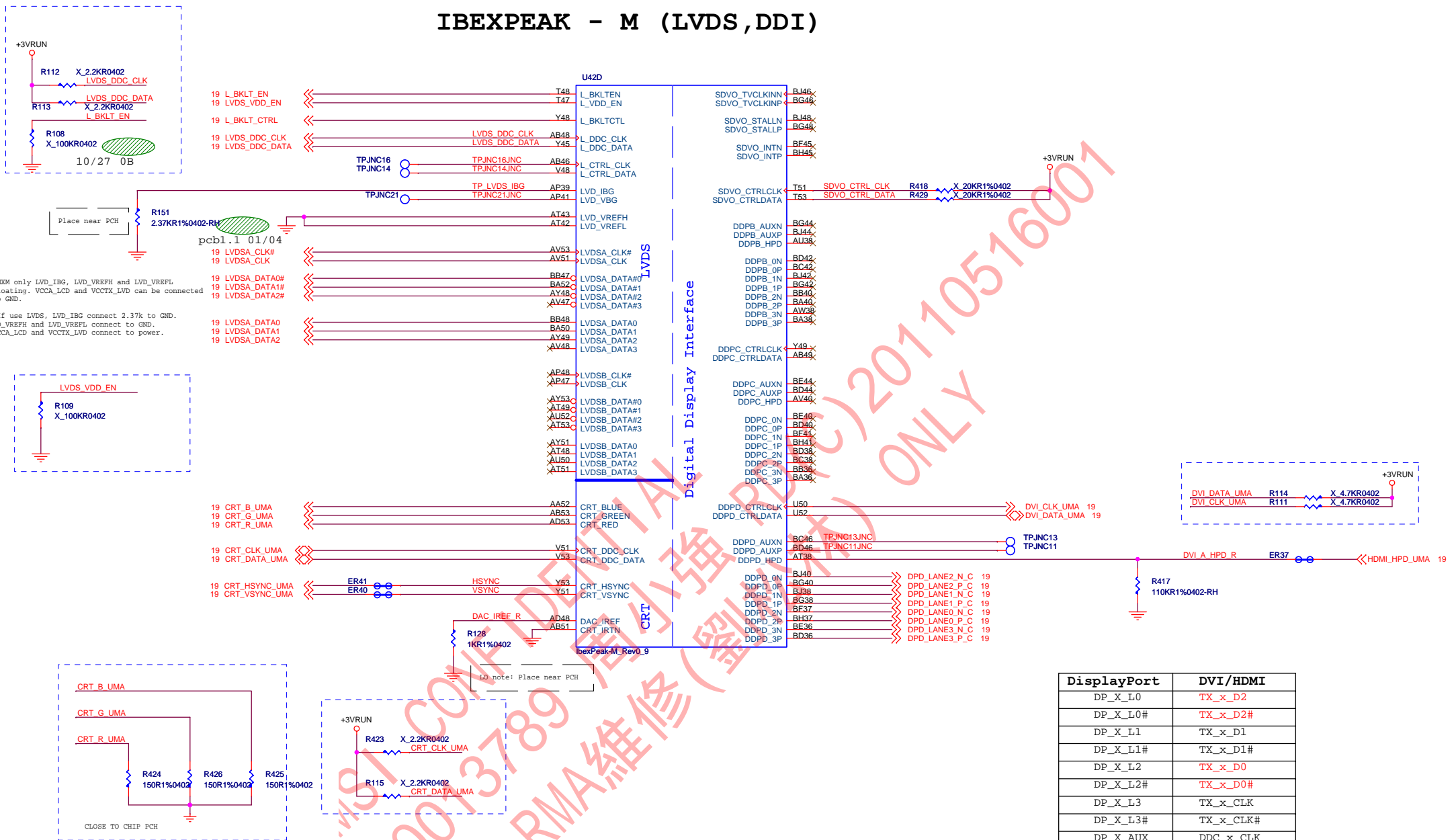


PCIECLKRQ1# / GPIO18 PCIECLKRQ1# / GPIO20	RUN Well
PCIECLKRQ0# and PCIECLKRQ3# ~ PCIECLKRQ7# PEG_A_CLKRQ# PEG_B_CLKRQ#	SUS Well

IBEXPEAK - M (DMI, FDI, GPIO)



IBEXPEAK - M (LVDS,DDI)

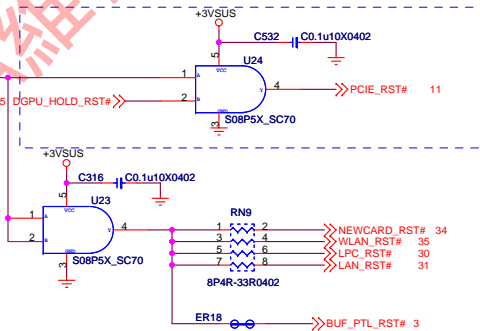
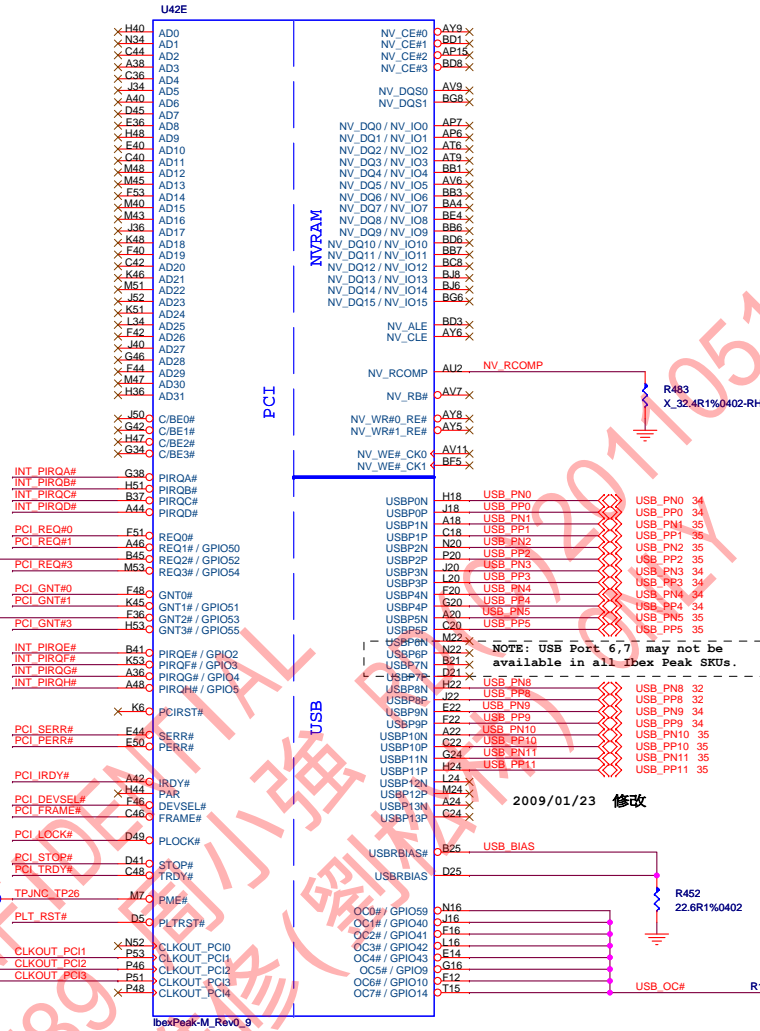
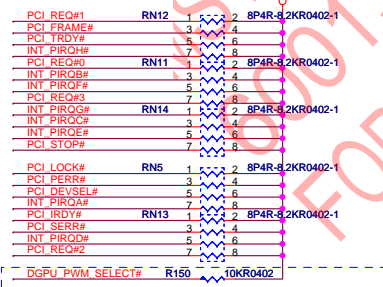
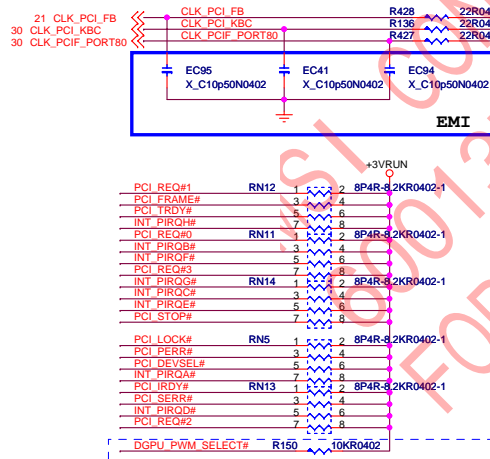
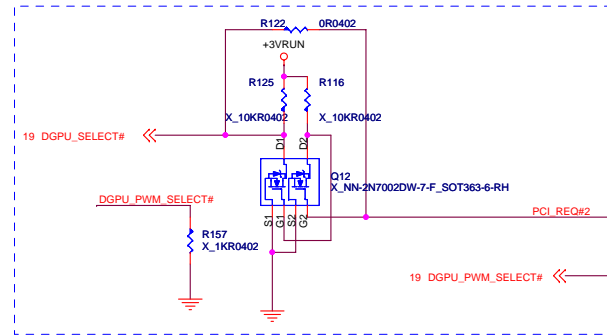


DisplayPort	DVI/HDMI
DP_X_L0	TX_x_D2
DP_X_L0#	TX_x_D2#
DP_X_L1	TX_x_D1
DP_X_L1#	TX_x_D1#
DP_X_L2	TX_x_D0
DP_X_L2#	TX_x_D0#
DP_X_L3	TX_x_CLK
DP_X_L3#	TX_x_CLK#
DP_X_AUX	DDC_x_CLK
DP_X_AUX#	DDC_x_DATA

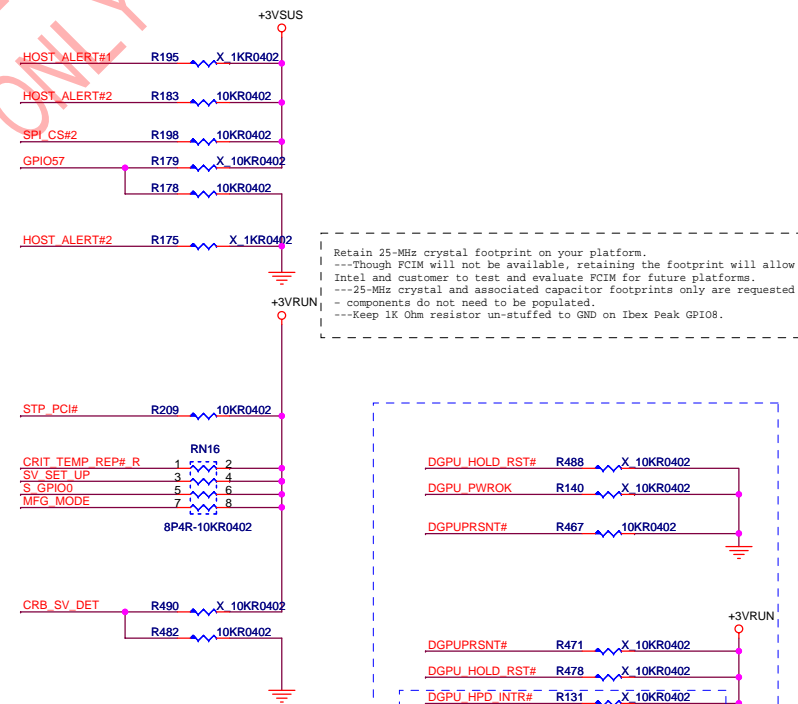
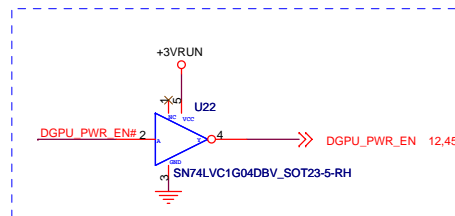
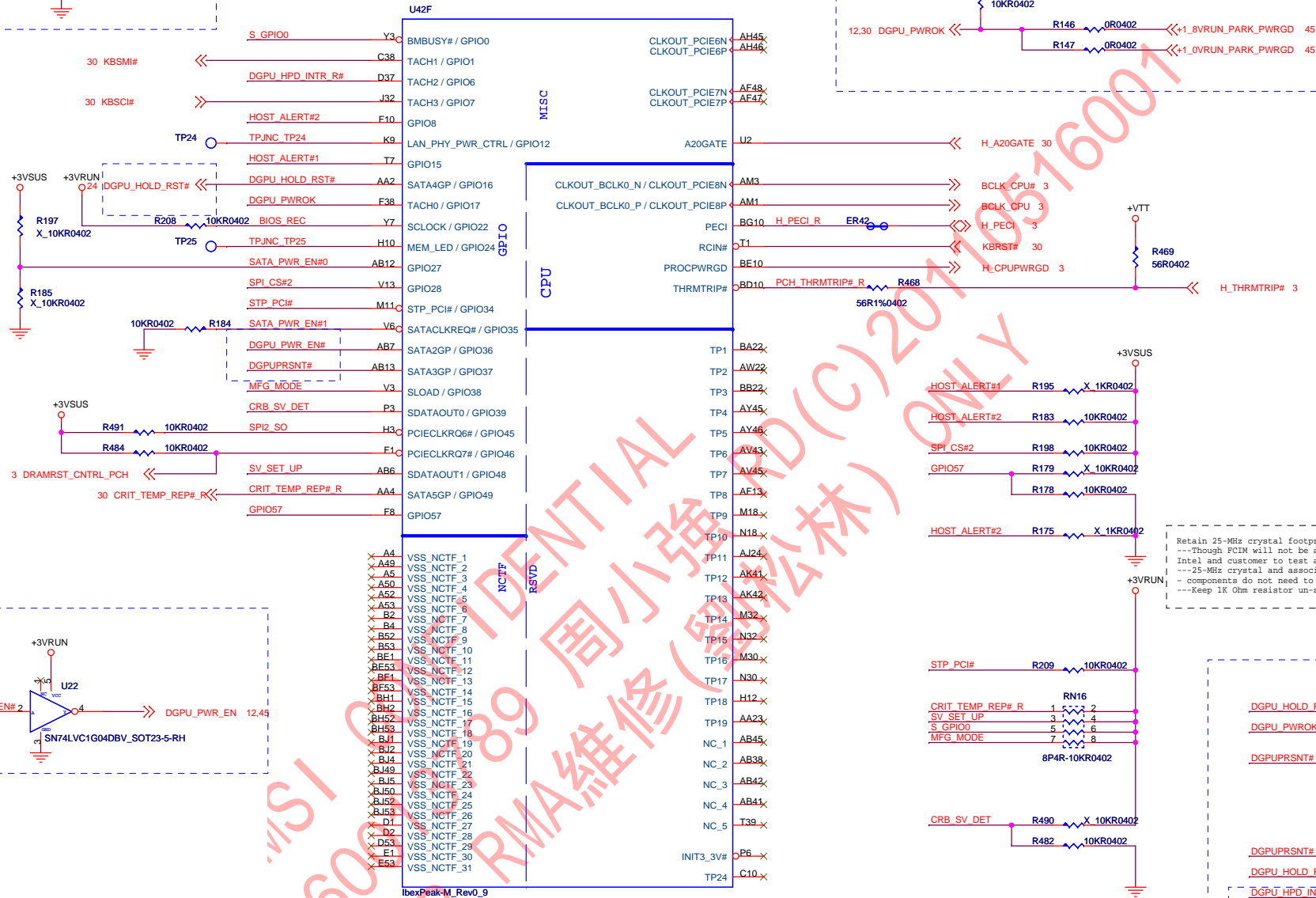
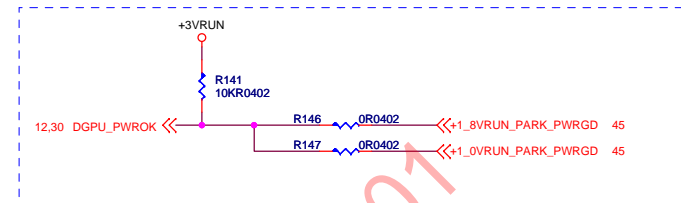
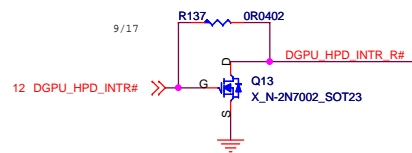
IBEXPEAK - M (PCI,USB,NVRAM)

Boot BIOS Strap		
PCI_GNT#0	PCI_GNT#1	Boot BIOS location
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPi

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default



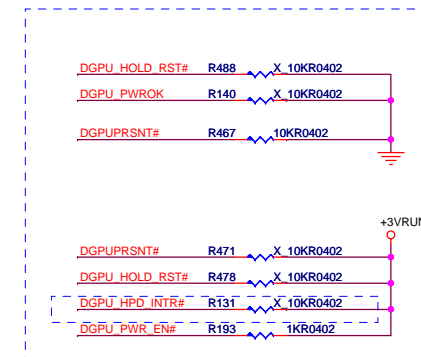
IBEXPEAK - M (GPIO,VSS_NCTF,RSVD)

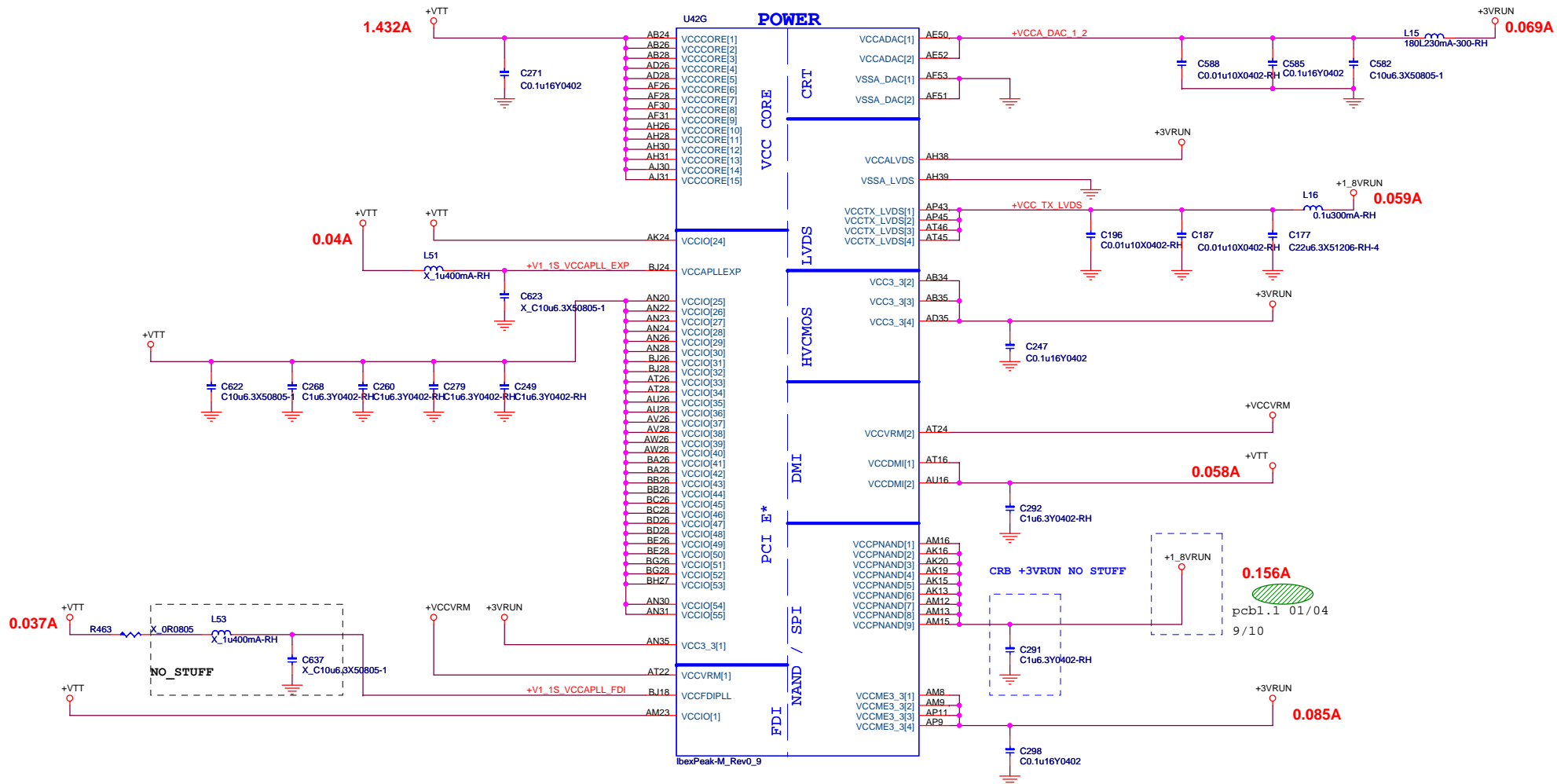


```

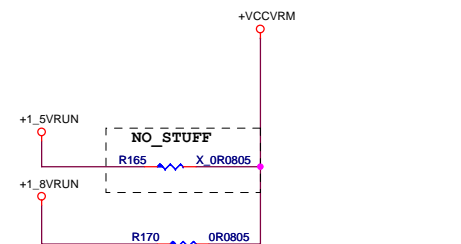
| Retain 25-MHz crystal footprint on your platform.
| ---Though FCIM will not be available, retaining the footprint will allow
| Intel and customer to test and evaluate FCIM for future platforms.
| ---25-MHz crystal and associated capacitor footprints only are requested
N| - components do not need to be populated.
| ---Keep 1K Ohm resistor un-stuffed to GND on Ibox Peak GPIO8.

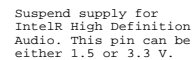
```



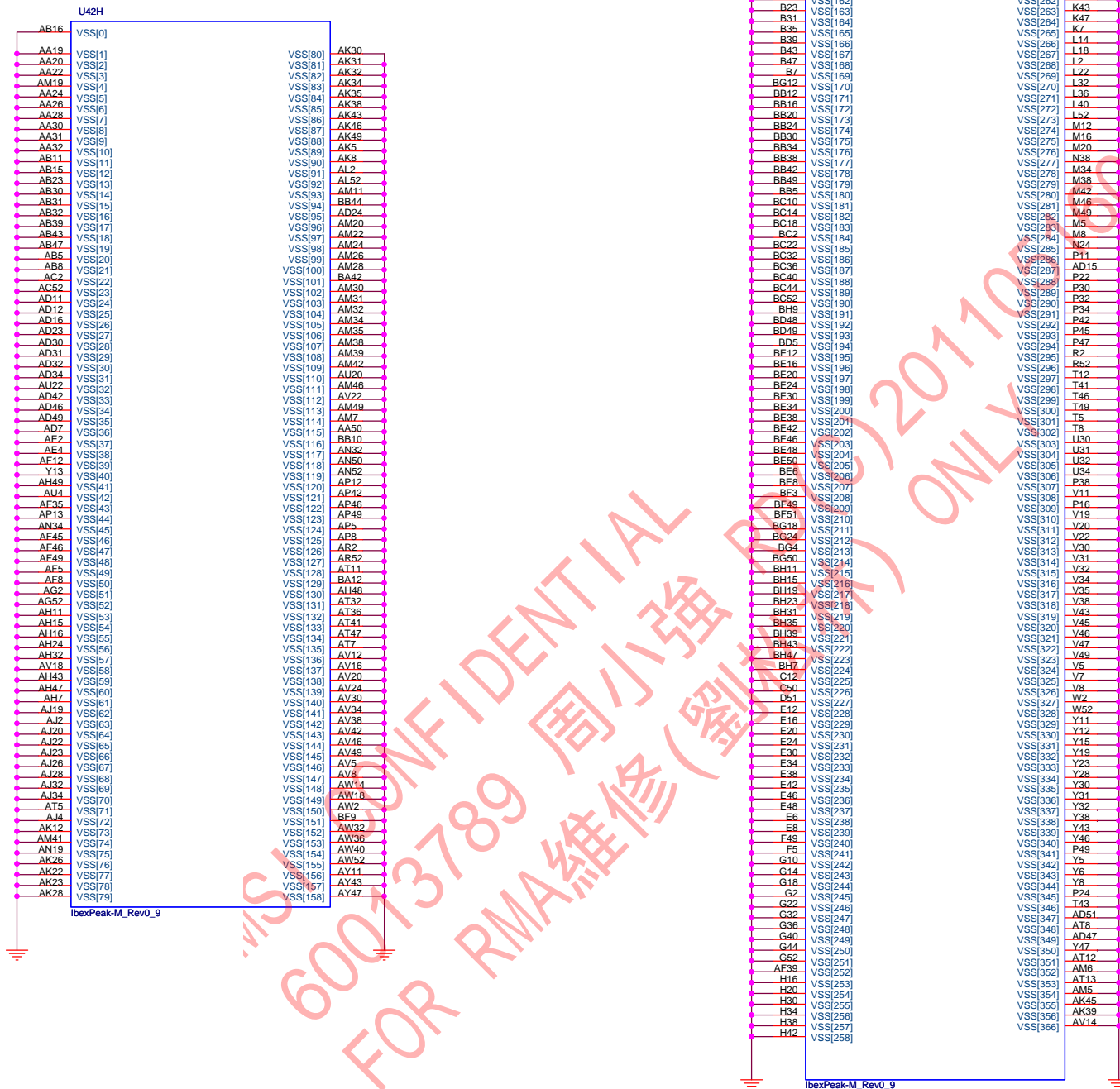
IBEXPEAK - M (POWER)

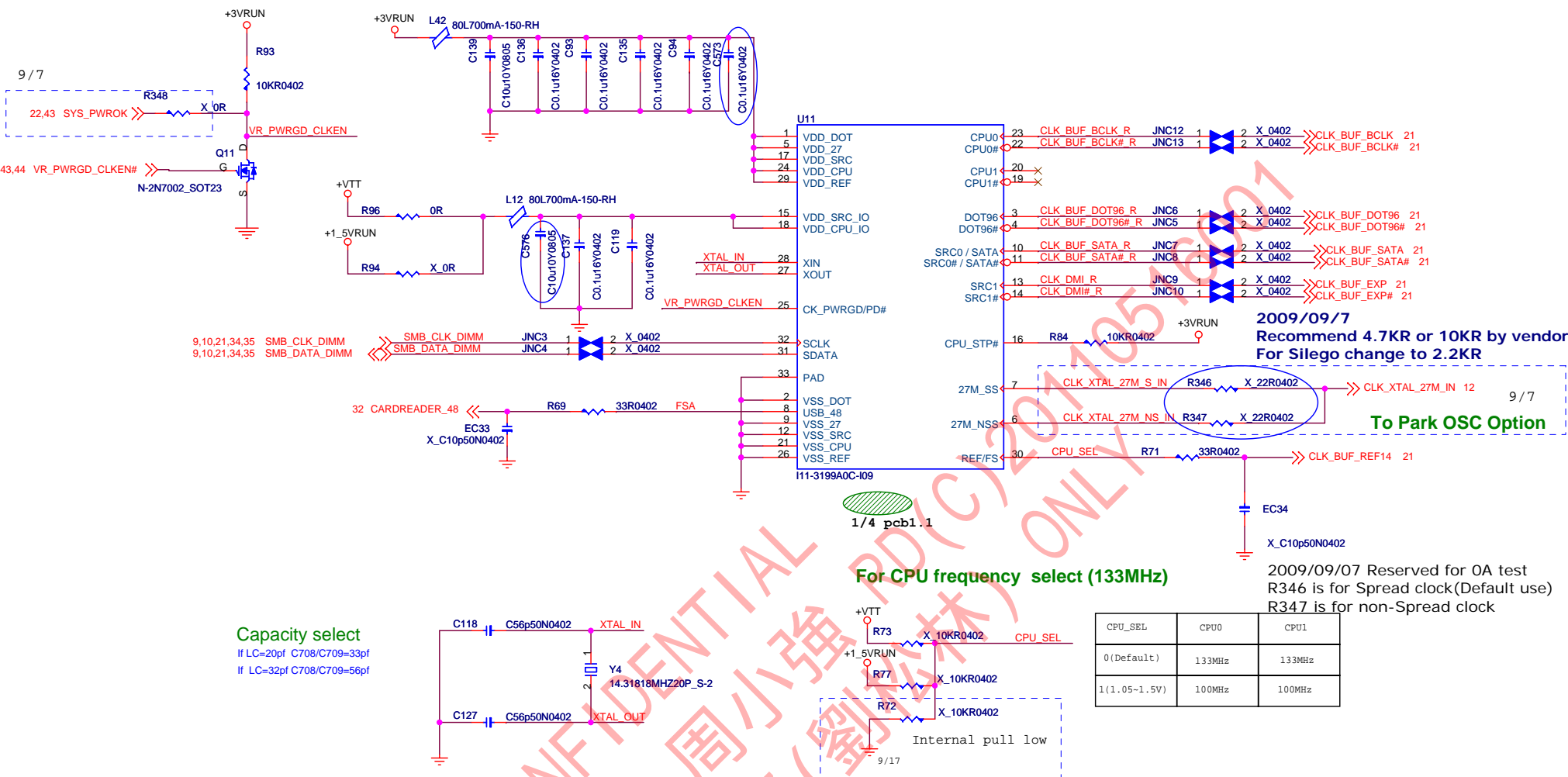
The VCCVRM rail (1.8 V/1.5 V) powers an internal voltage regulator module (VRM) that regulates clean 1.05-V voltage supply for analog rails (VCCAC1LK, Vccap11EXP, VCCFDIPLL, and VCCSATAPLL). This solution will allow us to remove the LC filter requirements for those rails, thereby reducing platform BOM cost. VCCVRM is enabled by default via internal pull up to GPIO27, therefore GPIO27 should be left as No Connect. The following diagram shows implementation details on how to enable and disable VccVRM.



IBEXPEAK - M (POWER)

IBEXPEAK - M (GND)





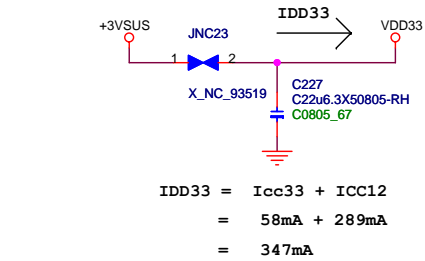
Capacity select
If LC=20pf C708/C709=33pf
If LC=32pf C708/C709=56pf

For CPU frequency select (133MHz)

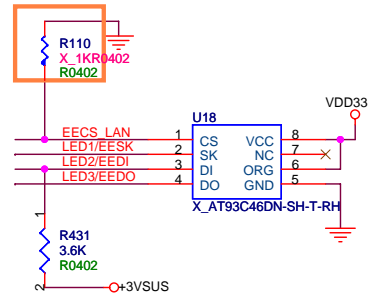
CPU_SEL	CPU0	CPU1
0(Default)	133MHz	133MHz
1(1.05~1.5V)	100MHz	100MHz

2009/09/7
Recommend 4.7KR or 10KR by vendor
For Silego change to 2.2KR

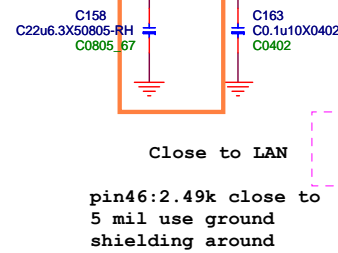
To Park OSC Option



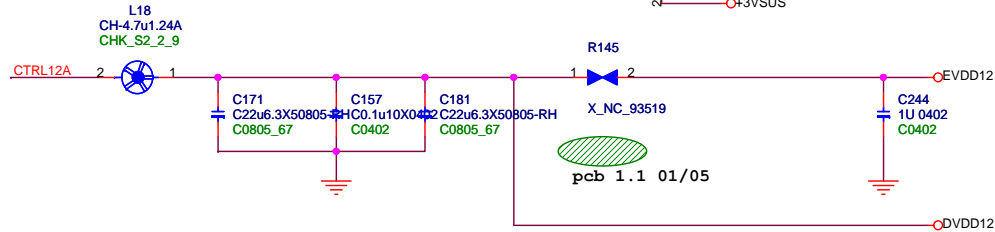
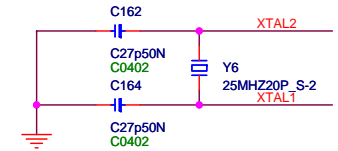
R110 is only required by RTL8102EL



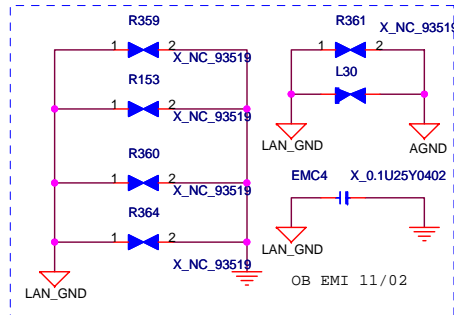
C158 is only RTL8111DL



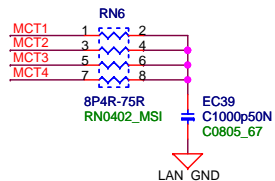
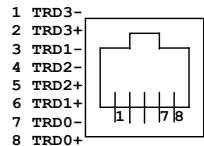
R106 is only RTL8111DL



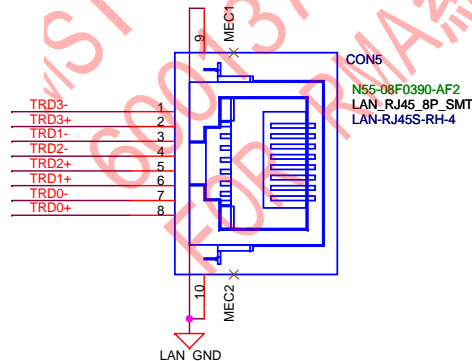
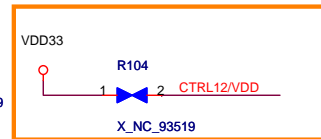
Note 1: The Trace length between L1 and 8111DL's Pin 1 must be within 0.5 cm. C171 and C181 to L18 must be within 0.5cm. Refer to Layout guide for more detail.



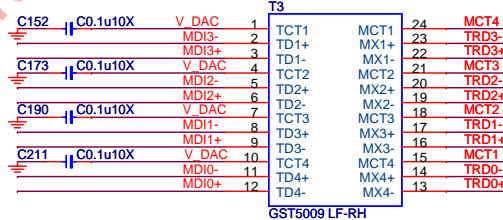
RJ45 Pin define



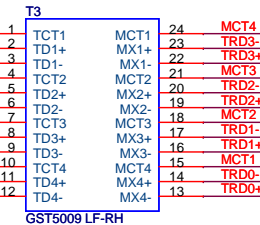
For RTL8111DL, use this block



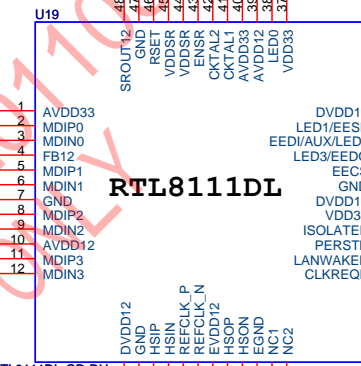
Close to Transformer



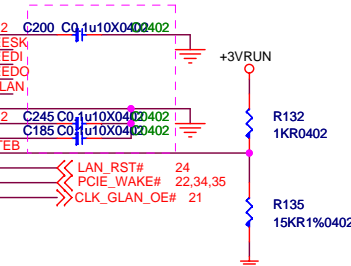
LAN MAGNETICS



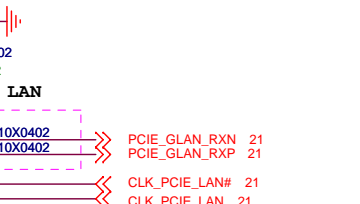
RTL8111DL



Close to LAN

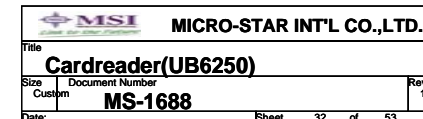


Close to LAN

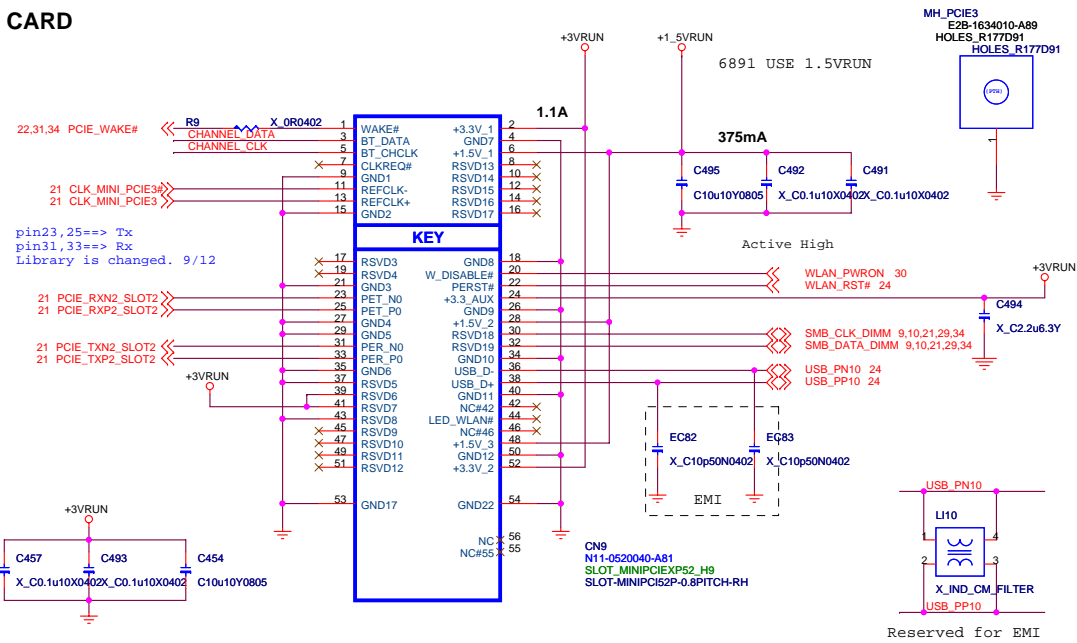


Close to LAN

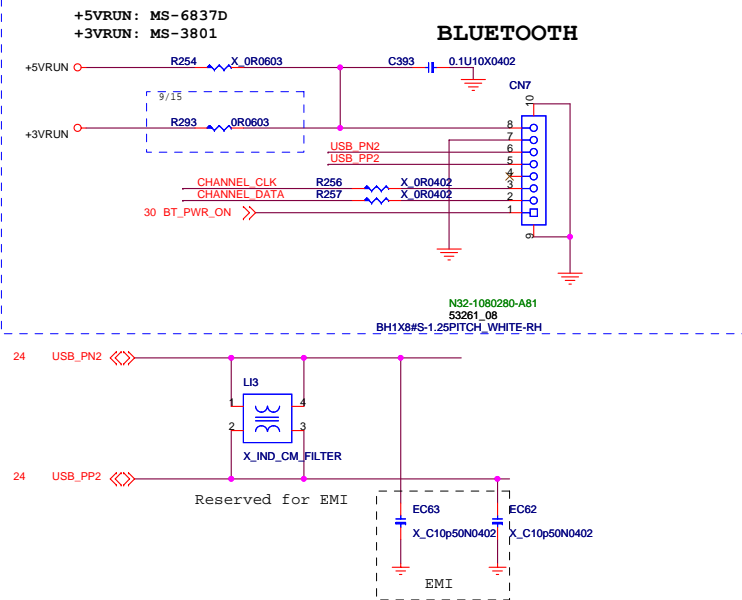




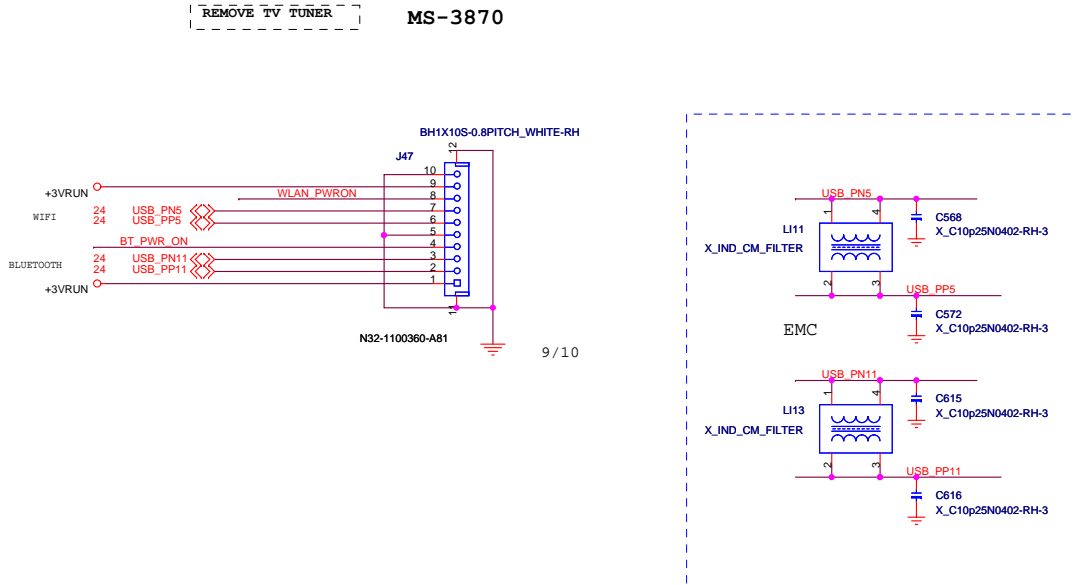
WLAN CARD



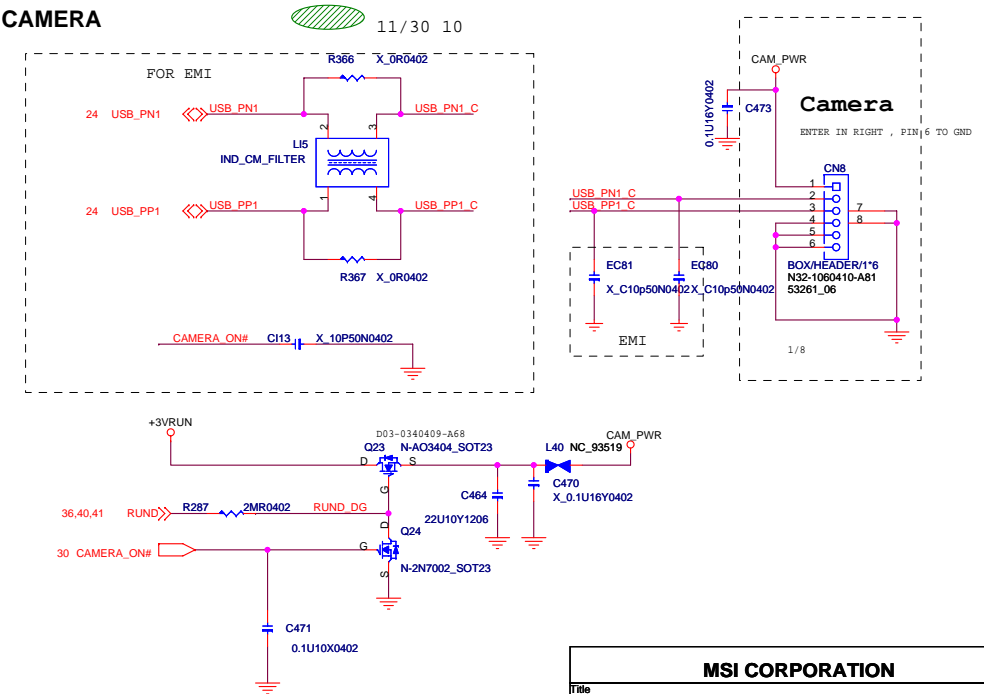
BLUETOOTH

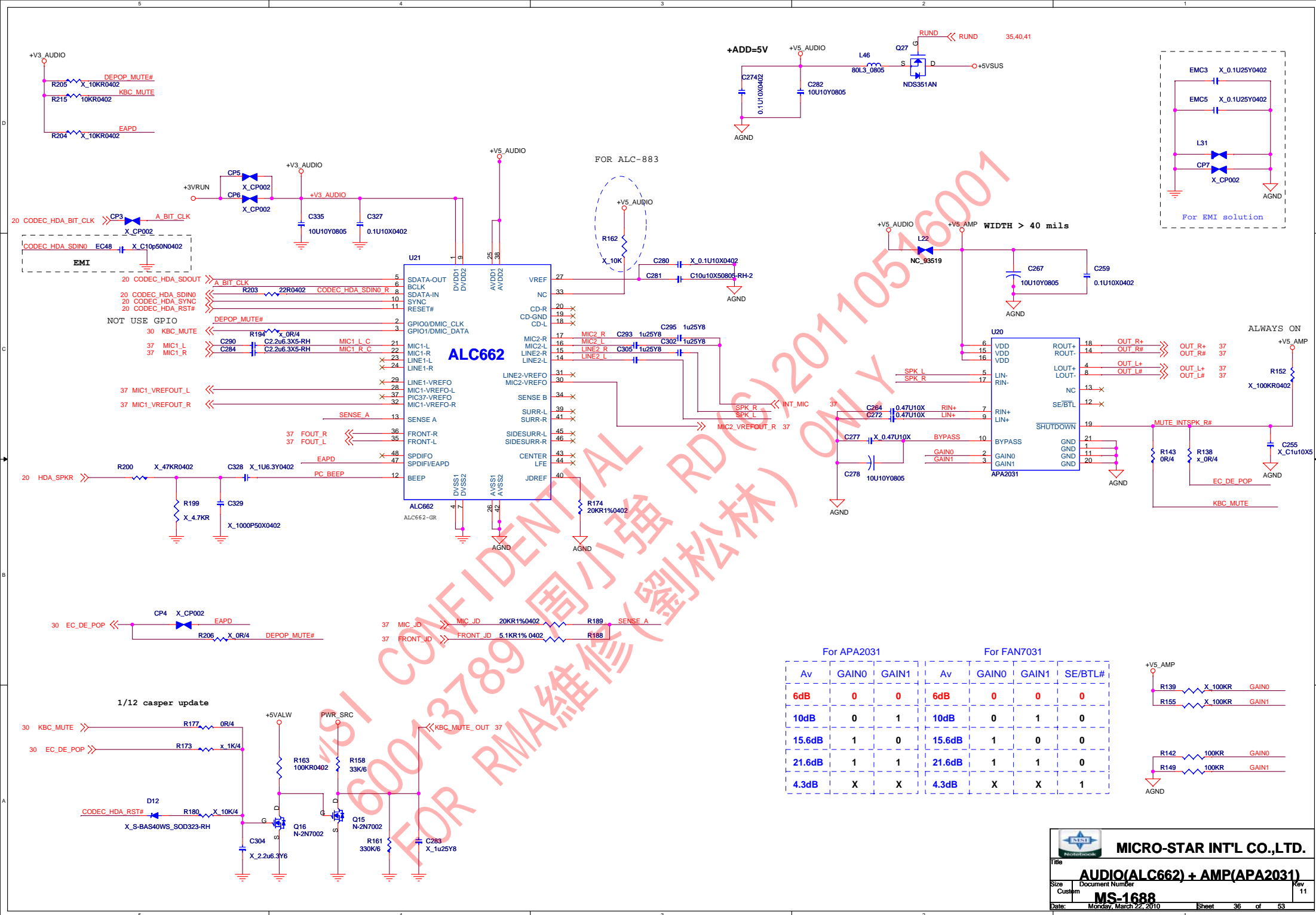


MS-3870



CAMERA





Power Management Section Schematic

Key Components and Connections:

- +3VRUN:** Connected to PQ18 (P-DTA114EKA_SOT23) and PQ8 (X_N-2N7002_SOT23-1).
- +3VALW:** Connected to PR182 (100KR0402) and PQ37 (NN-2N7002DW_SOT363-RH).
- +VCHG:** Connected to PQ10 (N-2N7002_SOT23) and PQ11A (PP-AO4805_S08).
- +VBATA:** Connected to PQ9A (PP-AO4805_S08) and PQ8A (PP-AO4805_S08).
- CHG_BATT_N:** Connected to PQ11B (PP-AO4805_S08) and PQ9B (PP-AO4805_S08).

Diode Specifications:

- Diode 1 (PQ11A):** I=8A, Is=2.6A
- Diode 2 (PQ11B):** I=8A, Is=2.6A
- Diode 3 (ES3BB):** I=8A, Is=2.6A
- Diode 4 (PD5):** I=8A, Is=3A

Resistor Values:

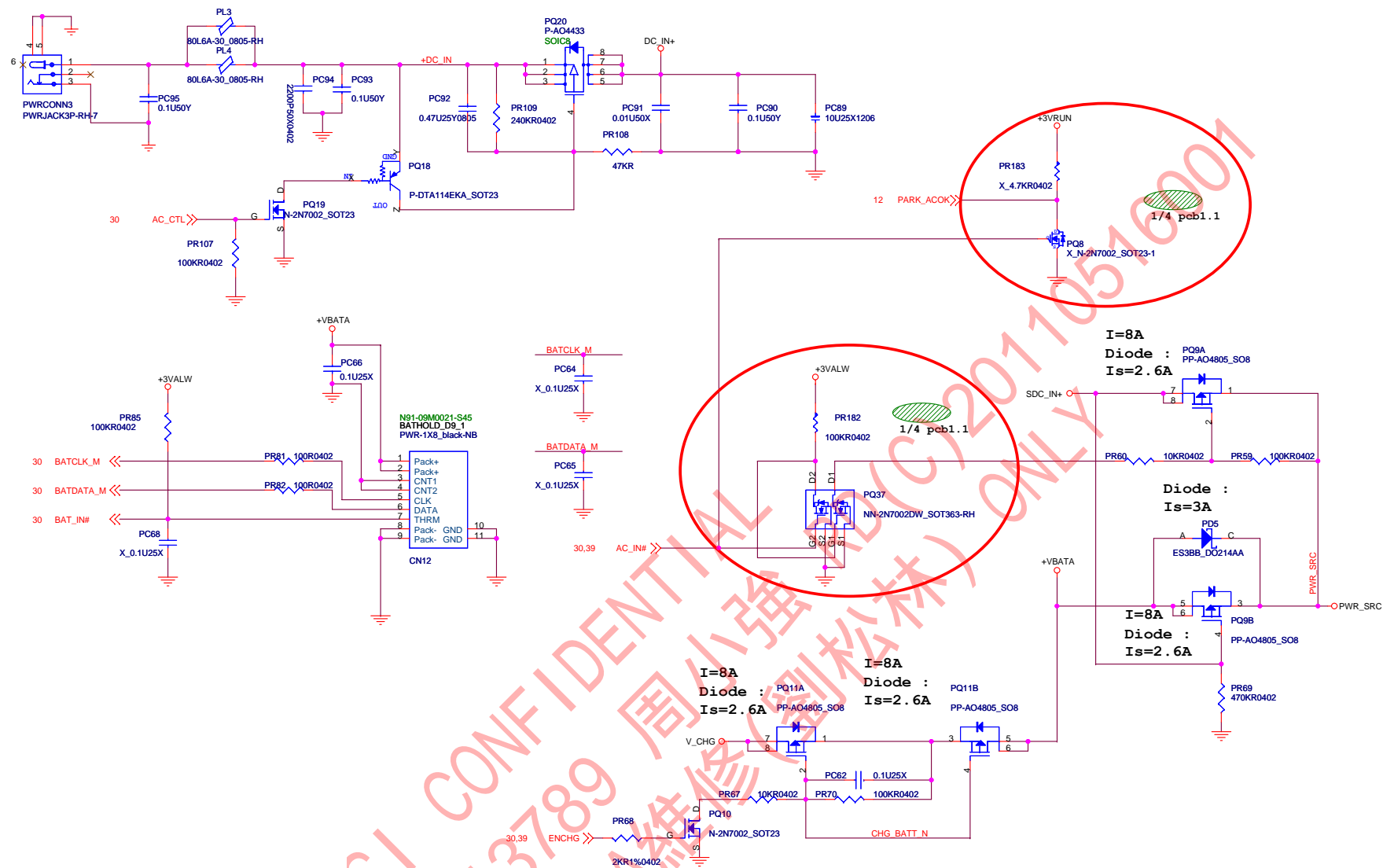
- PR108: 47KR
- PR182: 100KR0402
- PR183: X_4.7KR0402
- PR60: 10KR0402
- PR67: 10KR0402
- PR70: 100KR0402
- PR68: 2KR1%0402
- PC64: X_0.1U25X
- PC65: X_0.1U25X
- PC62: 0.1U25X
- PC66: 0.1U25X

Capacitor Values:

- PC64: X_0.1U25X
- PC65: X_0.1U25X
- PC62: 0.1U25X
- PC66: 0.1U25X

Other Components:

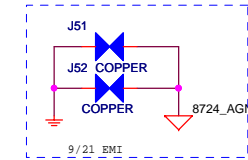
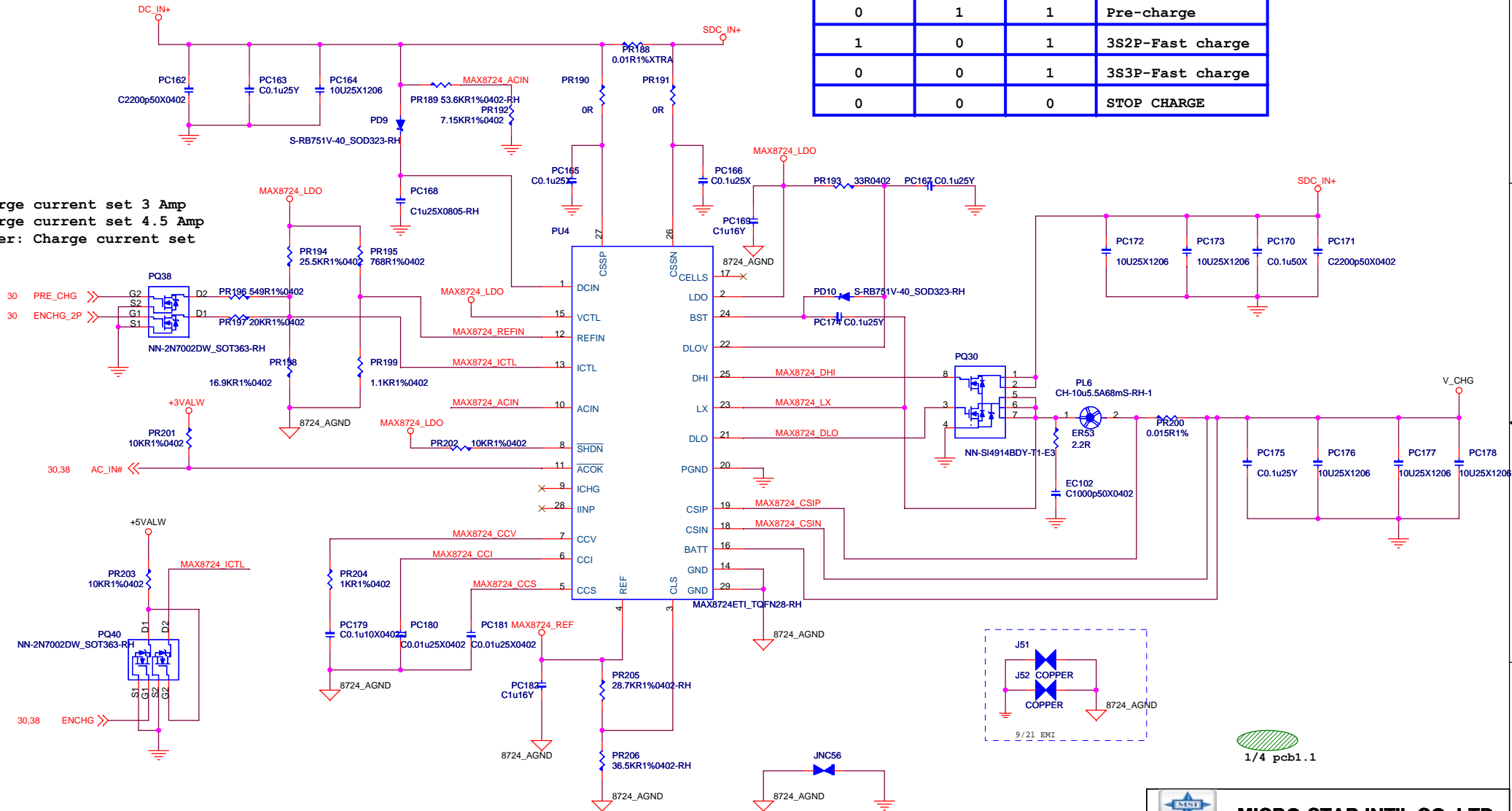
- PQ18: P-DTA114EKA_SOT23
- PQ10: N-2N7002_SOT23
- PQ37: NN-2N7002DW_SOT363-RH
- PQ9A: PP-AO4805_S08
- PQ8A: PP-AO4805_S08
- PQ9B: PP-AO4805_S08
- ES3BB: ES3BB_D0214AA
- PD5: PD5



Adapter= 90 W $2.048/7.15 \times (53.6+7.15)=17.4V$
 Adapter input voltage set 17.4 Voltage

ENCHG-2P	PRE_CHG	ENCHG	
0	1	1	Pre-charge
1	0	1	3S2P-Fast charge
0	0	1	3S3P-Fast charge
0	0	0	STOP CHARGE

3S2P: Charge current set 3 Amp
 3S3P: Charge current set 4.5 Amp
 Pre-charger: Charge current set 220mA



1/4 pcb1.1

MICRO-STAR INT'L CO.,LTD.

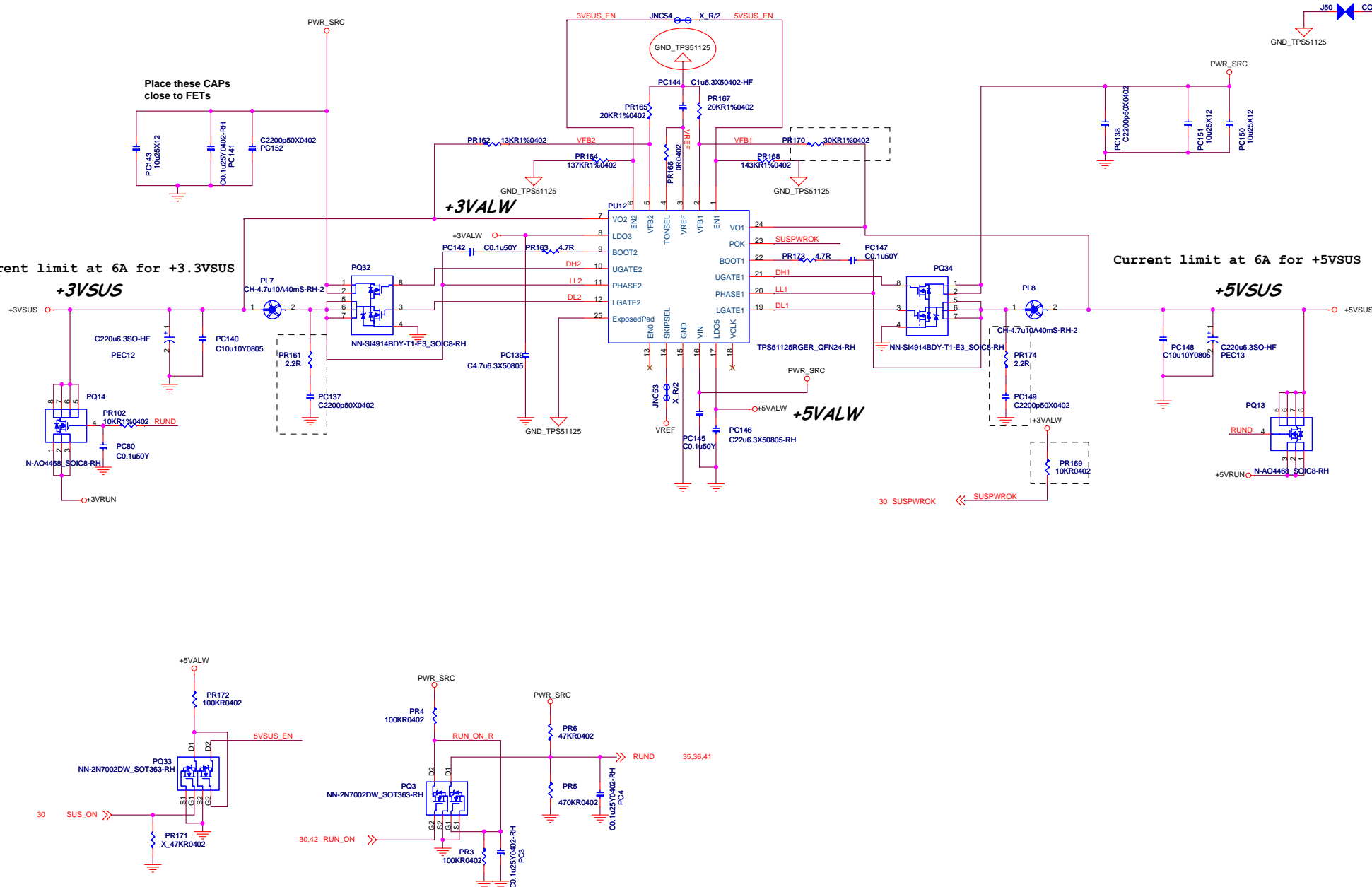
Battery Charger
E 51 / M 0

Size Custom Document Number **MS-1688** Rev 11

Date: Monday, March 22, 2010 Sheet 39 of 53

Current limit at 6A for +3.3VSUS

Current limit at 6A for +5VSUS



$$I_{LIM} = (R_{imax} \times 20\mu A / R_{dson}) + 1.82A$$

OCP 19A
MAX 14A

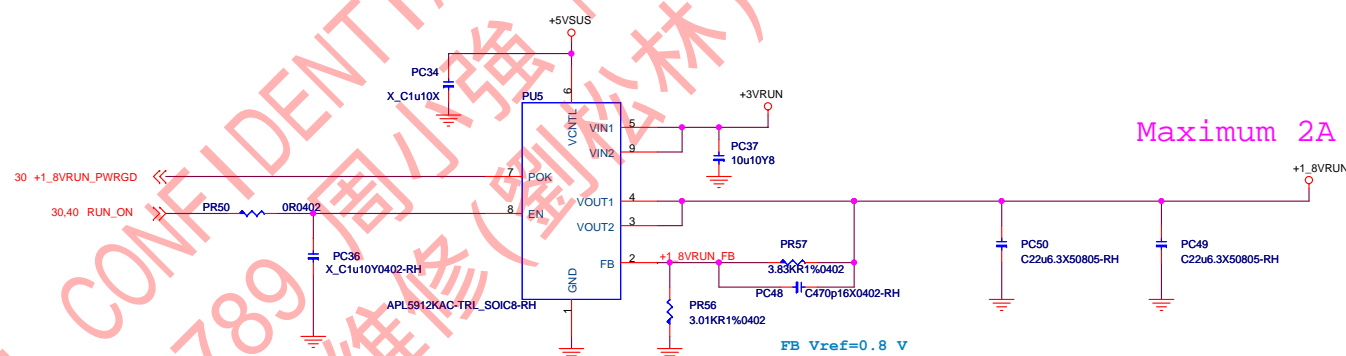
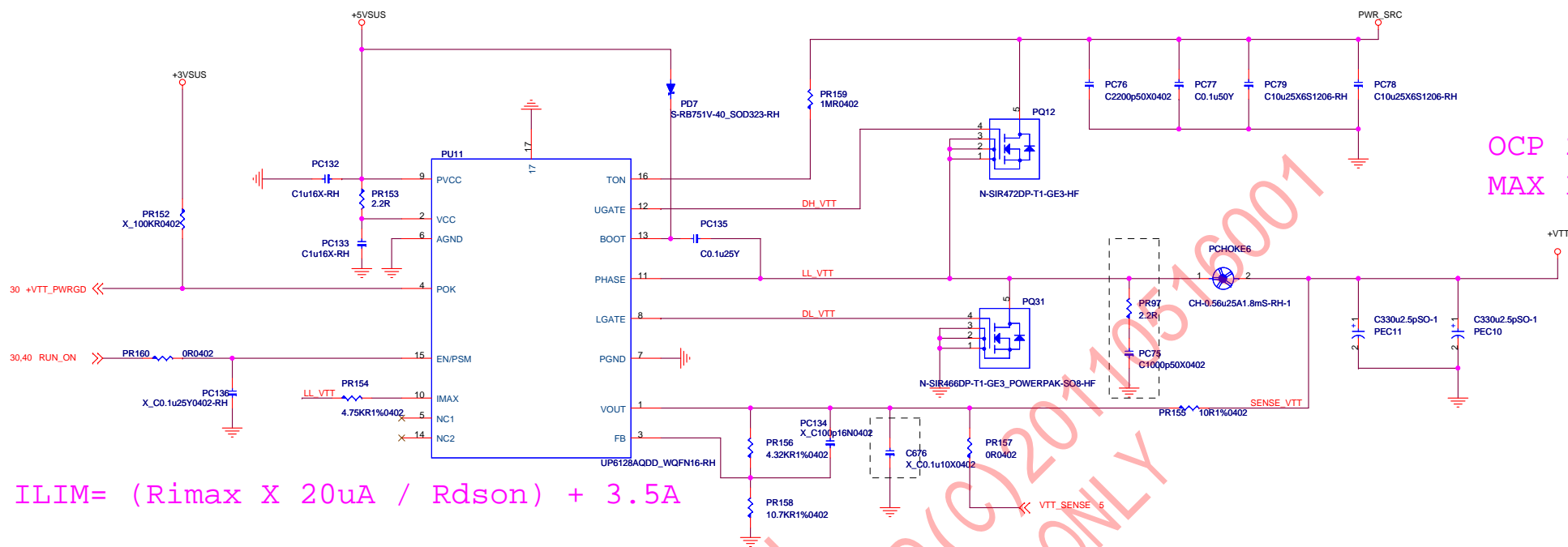
MAX 2A

8

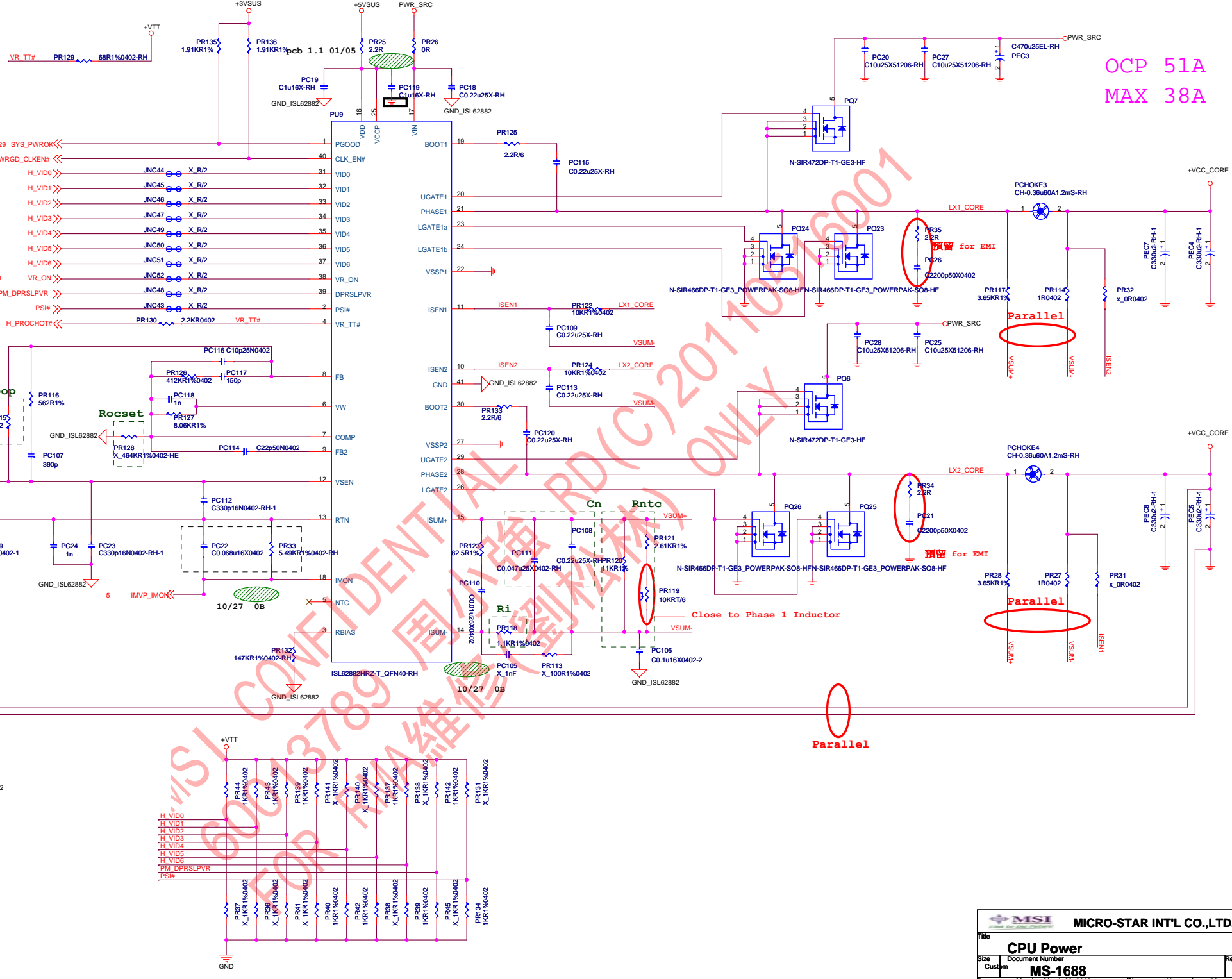
1

2

MSI MICRO-STAR INT'L CO.,LTD.			
Title	SMDDR VTERM /1 5VRUN		
Size	Document Number		Rev
Custom	MS-1688		11
Date:	Monday, March 22, 2010	Sheet	41 of 53



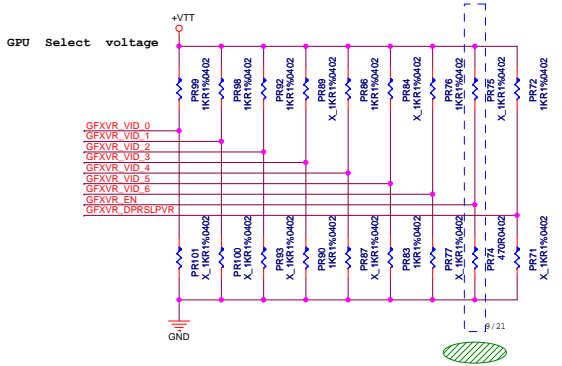
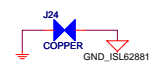
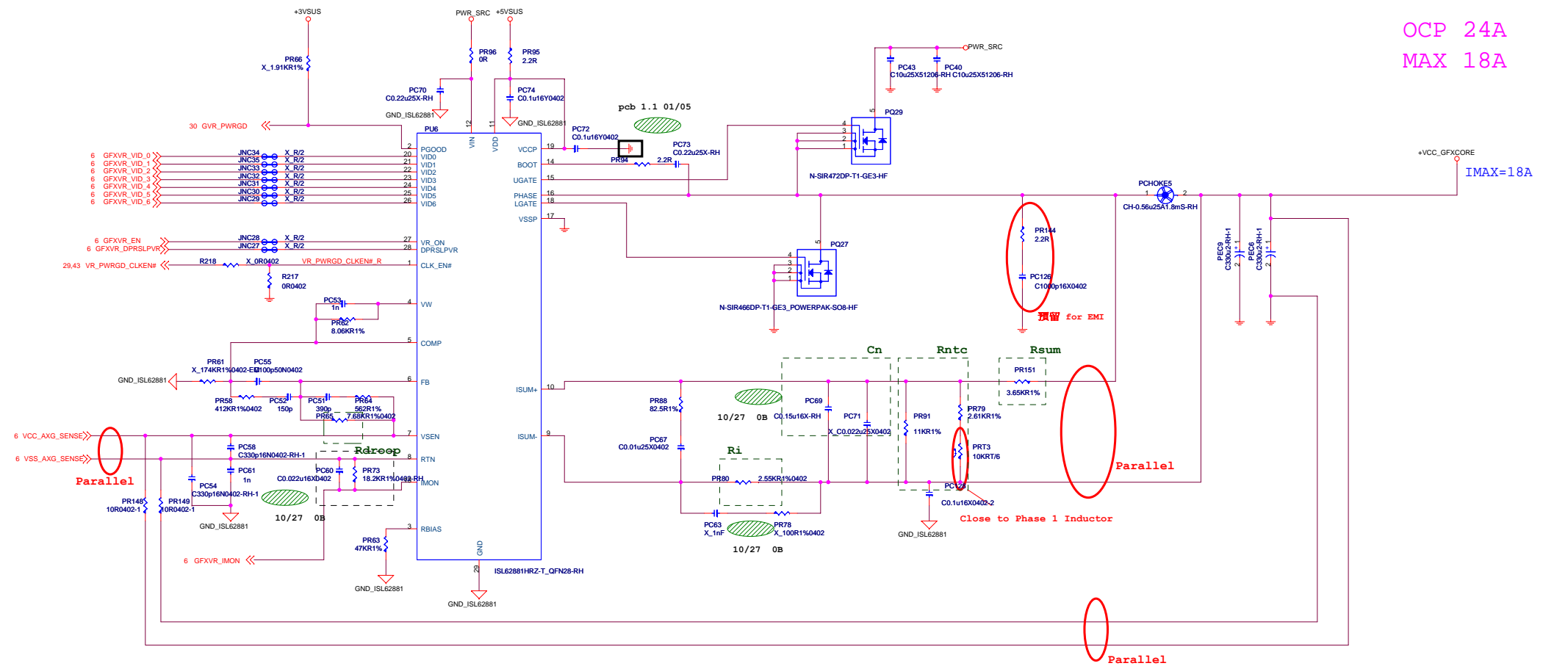
MSI MICRO-STAR INT'L CO.,LTD.			
Title			
VTT Power, +1.8VRUN			
Size	Document Number	Rev	
Custom	MS-1688	11	
Date:	Monday, March 22, 2010	Sheet	42 of 53

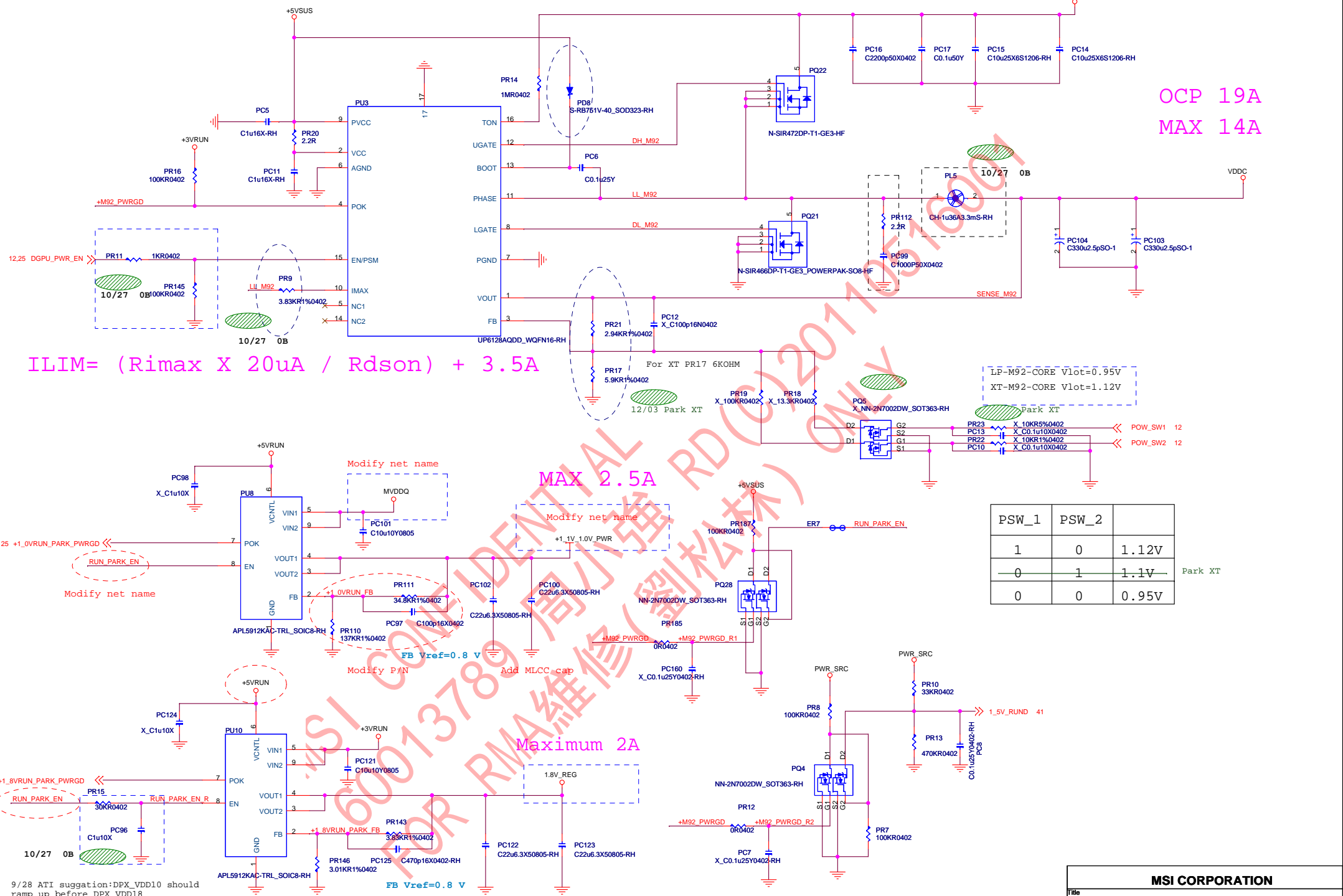


OCP 51A
MAX 38A

OCP 24A
MAX 18A

IMAX=18A



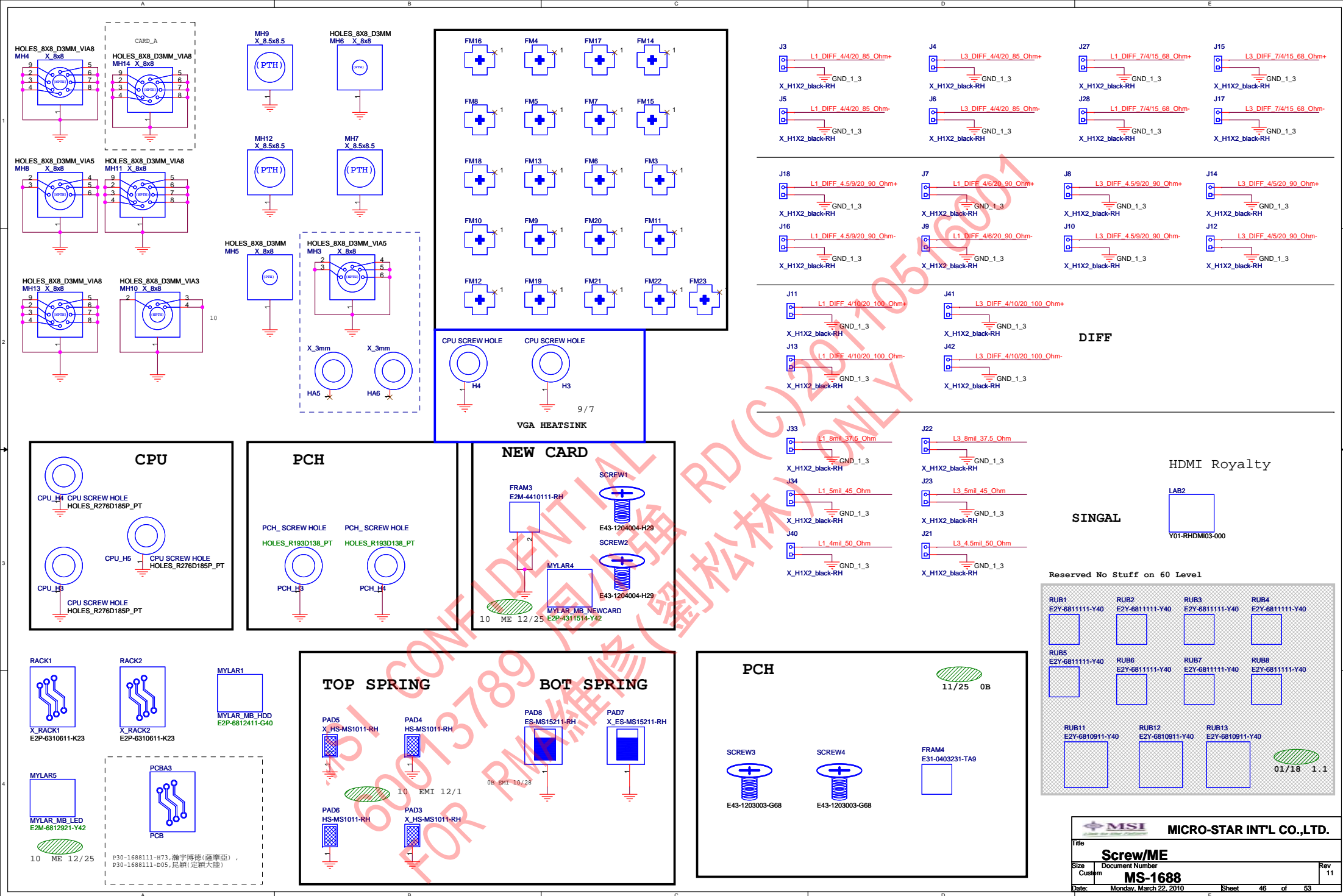


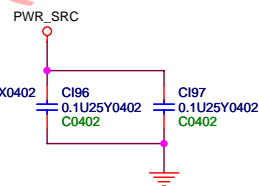
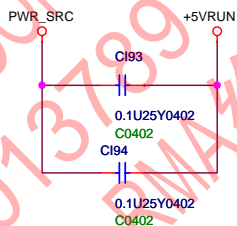
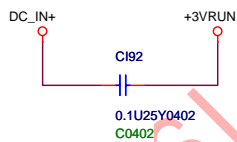
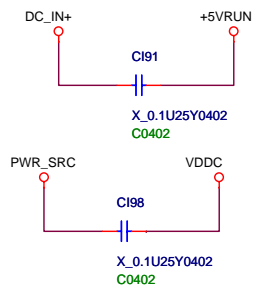
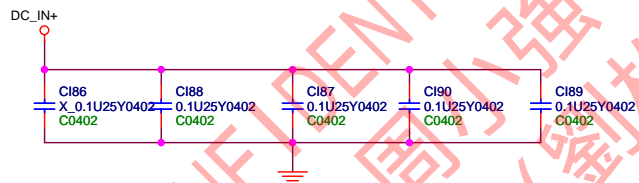
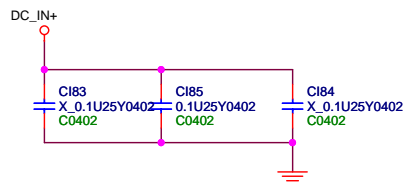
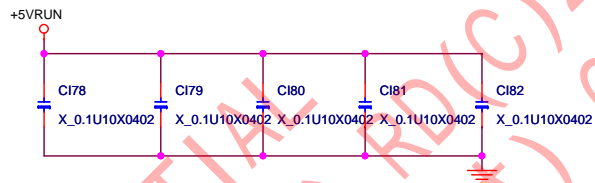
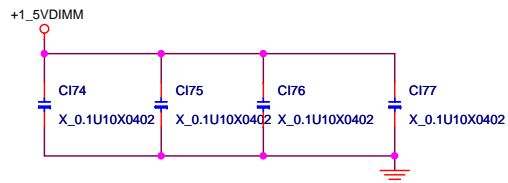
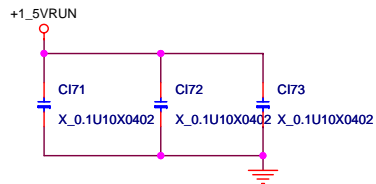
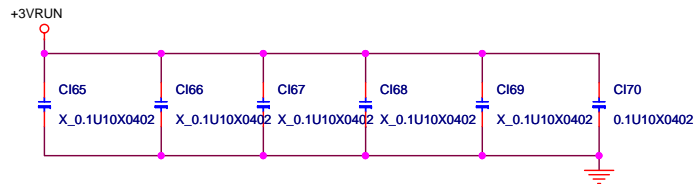
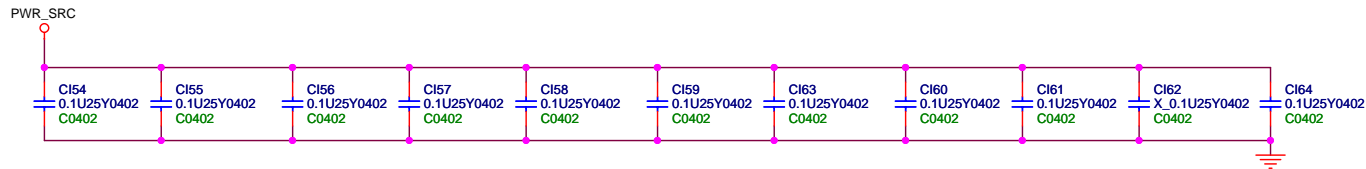
$$ILIM = (R_{imax} \times 20\mu A / R_{dson}) + 3.5A$$


PSW_1	PSW_2	
1	0	1.12V
0	1	1.1V
0	0	0.95V

Park XT

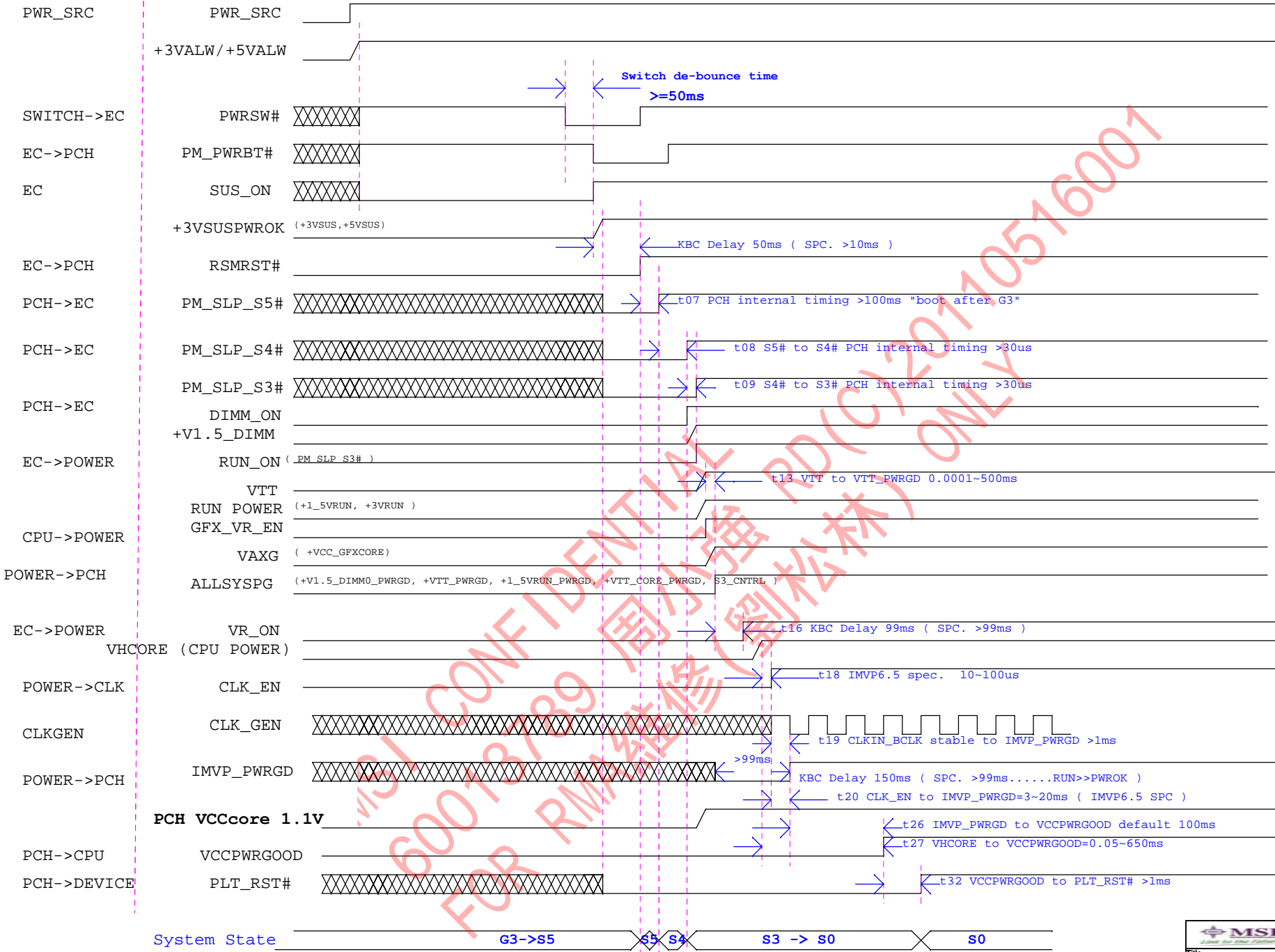
9/28 ATI suggestion:DPX_VDD10 should ramp up before DPX_VDD18



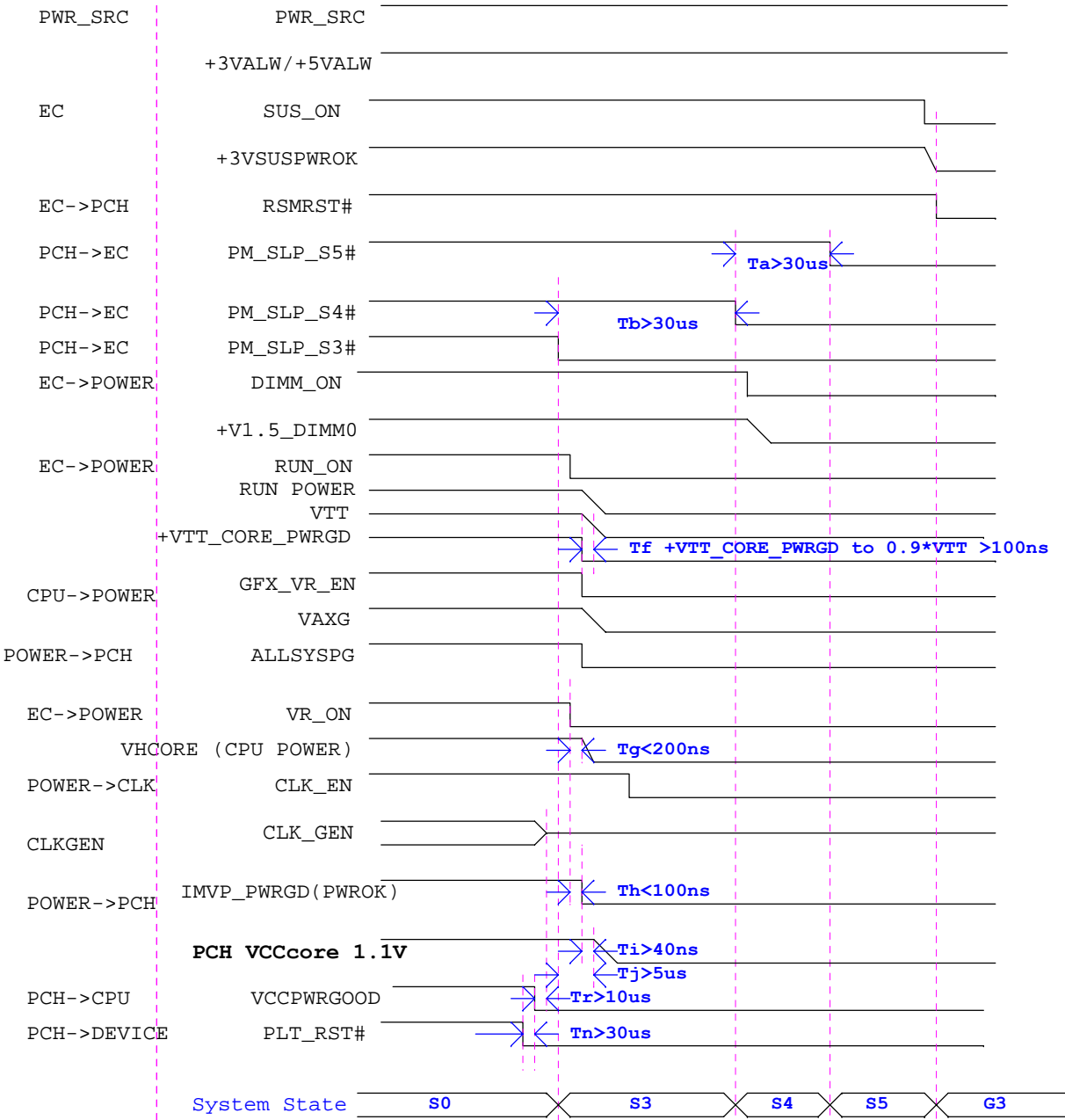


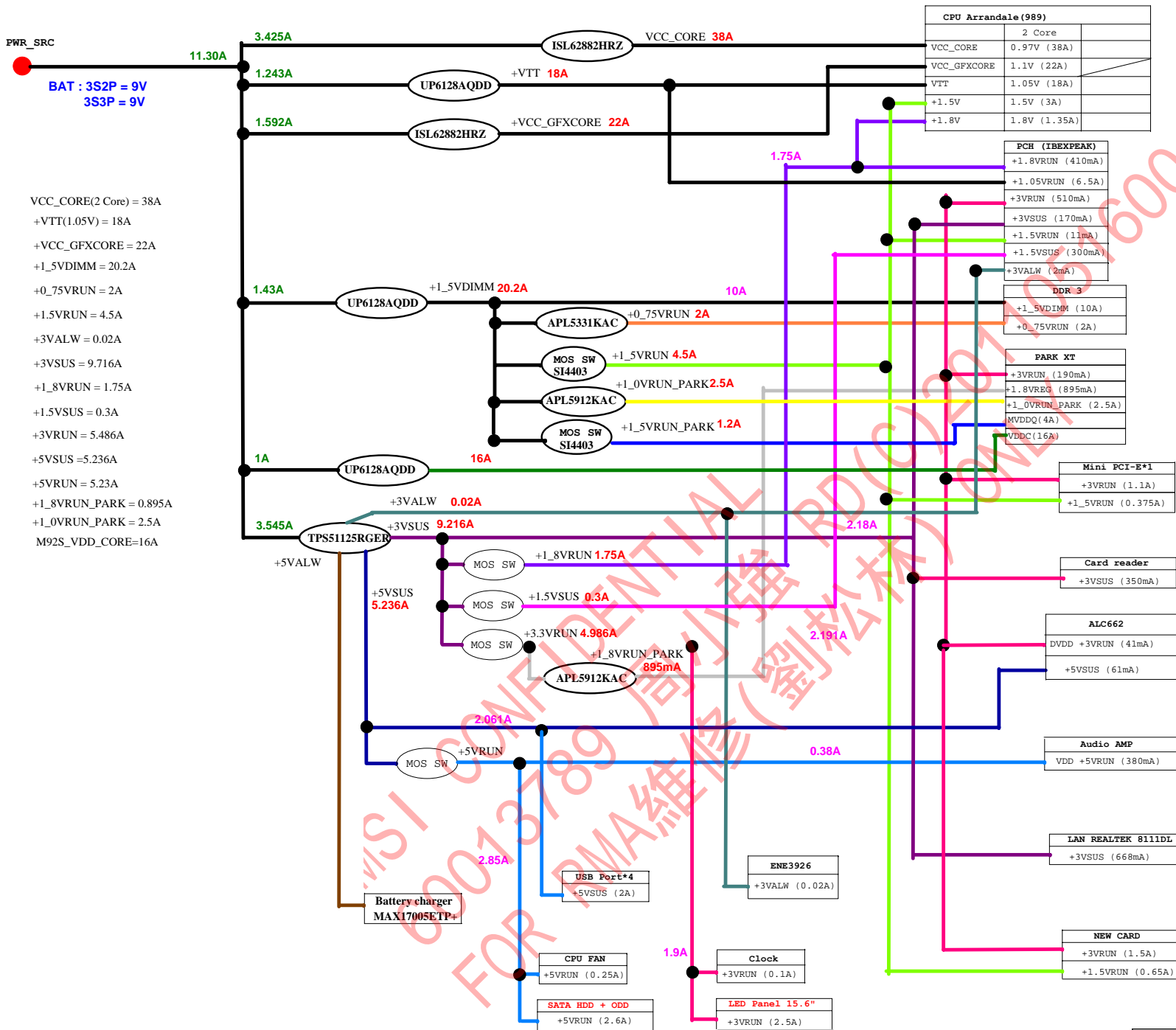
 MSI <i>Leading the Other Pathways</i>		MICRO-STAR INT'L CO.,LTD.	
Title			
EMI			
Size	Document Number		Rev
B	MS-1688		11
Date:	Monday, March 22, 2010	Sheet 49 of 53	

Calpella System Power on Sequence DC mode



Power down Sequence DC mode S0 to G3





0B

1. Page 13, Add R354, R356 0 ohm for Park VDDR4 connection
2. Page 14, Stuff R92 10K ohms for GPIO2 straps
3. Page 15, Remove R50, R315
4. Page 18, Change L33~35 for CRT RGB
5. Page 19, Change D4 to BAS40 for HDMI testing
6. Page 20, Remove BIOS1 socket
7. Page 20, Add R581 1K ohms for PCH GPIO33 to EC GPIO13 connection and remove R159
8. Page 20, Change C634, C640 to 15pF
9. Page 23, Remove R108
10. Page 30, Change CON6 to vertical type for debug card
11. Page 33, Remove Q5, Q14 for Power switch LED and change R15 to 0 ohm
12. Page 34, Change J43 to eSATA connector and add C594~596, C698, C699 for eSATA solution, Remove C462
13. Page 34, Add U45, U46, C702, C704, R353, R362 for USB power protect switch and remove F4, F5
14. Page 38, Change PR183 to 4.7K to reduce the drop voltage
15. Page 39, Stuff ER46, EC102 for V_CHG
16. Page 40, Stuff PR161, PC137 for +3VSUS, PR174, PC149 for +5VSUS
17. Page 41, Stuff R247 1K ohms, No stuff R518, Change PR179 to 10.5K, R517 to 200K
18. Page 41, Stuff PR105, PC88 for +1_5VDIMM
19. Page 42, Stuff PR97, PC75 for +VTT
20. Page 43, Stuff PR35, PC26, PR34, PC21 for +VCC_CORE
21. Page 43, Change PC22 to 0.047uF, PR33 to 8.06K, PR115 to 2.32K, PR118 to 1.1K
22. Page 44, Stuff PR144, PC126 for +VCC_GFXCORE
23. Page 44, Change PC60 to 0.022uF, PC69 to 0.15uF, PR65 to 7.68K, PR73 to 18.2K, PR80 to 2.55K
24. Page 45, Change PR9 to 3.83K
25. Page 45, Stuff PR112, PC99 for VDDC and change PL5 to 1uH for reduce noise
26. Page 45, Change PR15 to 30K and stuff PC96 1uF for 1.8V_REG delay 1.2mS after +1_1V_1.0V_PWR
27. Page 45, Change PR11 to 1K and stuff PR145 100K to reduce current leakage
28. Page 46, Stuff PAD8 for EMI and add SCREW1, 2 in BOM. Remove BRACKET1
29. Page 49, Stuff CI54~64, CI70, CI85, CI87~90, CI92~97 for EMI
30. Page 16, Add PC158, PC161, Reserve C700, C701 for MVDDQ
31. Page 12, Add ATI debug point
32. Page 31, Add EMI cooper to seperate LAN GND
33. Page 32, Reserve R365 for cardreader issue
34. Page 45, Stuff PR18 13.3K, PQ5, PR23 10K for Park XT

10

1. Page 12, No stuff R118; stuff R220,R210,R169 for ATI PARK SAMPLE
2. Page 16, Remove C701 location, No stuff C64 for DFM
3. Page 16,page17, modify R322,R318,R51,R49,R324,R321,R320,R316 to 121R ohm for 3D device lost
4. Page 19, Add R11, R13, R20, R22 for GPU switch issue
5. Page 19, Add C705, C706 5pF0402 for EMI
6. Page 29, stuff R347 for ATI PARK sample
7. Page 32, Reserve R400 for ene S3 resume issue
8. Page 33, Change R26, R29 location name (Org. is R11, R13) and change the footprint to NC_0402_6
9. Page 34, Stuff CMC L3, L4 for EMI
10. Page 35, Stuff CMC LI5 for EMI, and reserve R366, R367
11. Page 44, PR74 change to 470ohm for intel ww48
12. Page 45, unstuff PR19 PQ5 PR22 ,PR17 change to 5.9Kohm fix =1.12vlot,stuff PC103 for PARK--XT
13. Page 47, Stuff CMC LIA3 for EMI, and reserve R368, R369
14. Page 48, Stuff CB3~7, JNCB3~7 for ESD
15. Page 46, Stuff PAD4, PAD6 for ESD, Add Fram4, SCREW3, SCREW4
16. Page 46, ADD mylar4;mylar5 for newcard and led ESD

11

1. page 6 remove R506;page 11 R434,R435 modify cooper;page 12 remove R95,R522,R399,R406,R407 ; page 13 unstuff R354,R356
2. page 15 remove R76,R70;page 19 stuff R11,R13,R20,R22,;unstuff R81,U14,C113
3. page 23 remove R148,R144;page 26 remove R192
4. page 29 modify pn:SLG28770ELC
5. page 30 add GPIO3F :2P_CHG;GPIO0D MB/ID;GPXIOA06:PRE_CHG;AC_OK change to AC_IN#;modify R351 to cooper
6. page 31 reomove R106,R103,R133;modify R145,R104 to cooper
7. page 32 reomove R223;page 34 remove R353,R352,R362,R363
8. page 38 modify AC_OK to AC_IN#
9. page 39 modiy MAX 8724 charge IC
10. page 43 ,page44 modiy PC119 ,PC72 to digital GND
11. page 49 ,No Stuff CI62
12. page 32 ,Change U25 PN to Ver:A3
13. page 46 ,Add Rubber Rub1~8, Rub11~13 to 60 level for IE request

2010/03/11 Add BIOS Lable, HDMI Royalty, MS-1688B switch change to 4.9mm

MSI CORPORATION			
Title			
Change Histoy			
Size	Document Number		Rev
Custom	MS-1688		11
Date:	Monday, March 22, 2010		Sheet 53 of 53